

# Enrico/Caruso 15" UMA Schematics Document

## rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2011-04-22

[www.aitech1.ru](http://www.aitech1.ru)

REV : A00

*DY : Nopop Component*  
*HDMI : Pop for HDMI function*  
*No\_HDMI : Pop for NO HDMI function*  
*10/100 : Pop for 10/100 LAN*  
*GIGA : Pop for GIGA LAN*  
*Surge : Pop for surge option*  
*G709 : Pop G709 thermal solution*  
*INS : Pop for Inspiron series ID*  
*VOS : Pop for Vostro series ID*  
*S3 : Pop for S3 power reduction*  
*Normal : Pop for NO S3 power reduction*

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**Enrico/Caruso 15 CP**

Rev  
A00

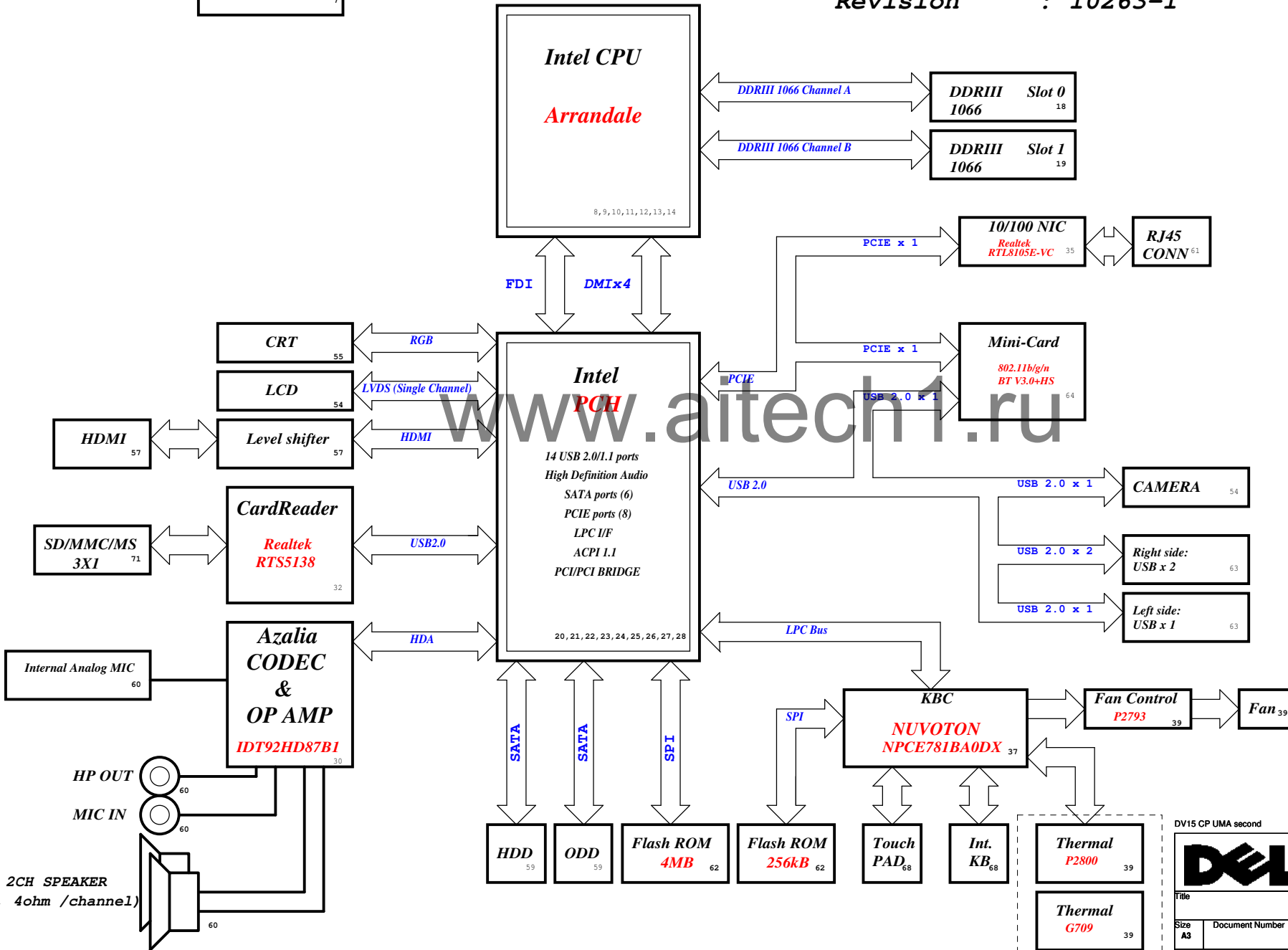
Date: Friday, April 22, 2011

Sheet 1 of 99

# DV15 Calpella UMA Block Diagram

Project code : 91.4IP01.001  
PCB P/N : 48.4IP01.011  
Revision : 10263-1

Clock Generator  
**SLG8SP595**



MAXIM CHARGER	
BQ24707 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
TPS51123 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +3.3V_ALW +5V_ALW +15V_ALW
CPU DC/DC	
ISL62882 47, 48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
RT8237A 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_CPU +1.05V_PCH
SYSTEM DC/DC	
RT8207 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +V_DDR_REF +0.75V_DDR_VTT
SYSTEM DC/DC	
APW7153B 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_CPU +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top L2: GND L3: Signal L4: Signal L5: VCC L6: Bottom	

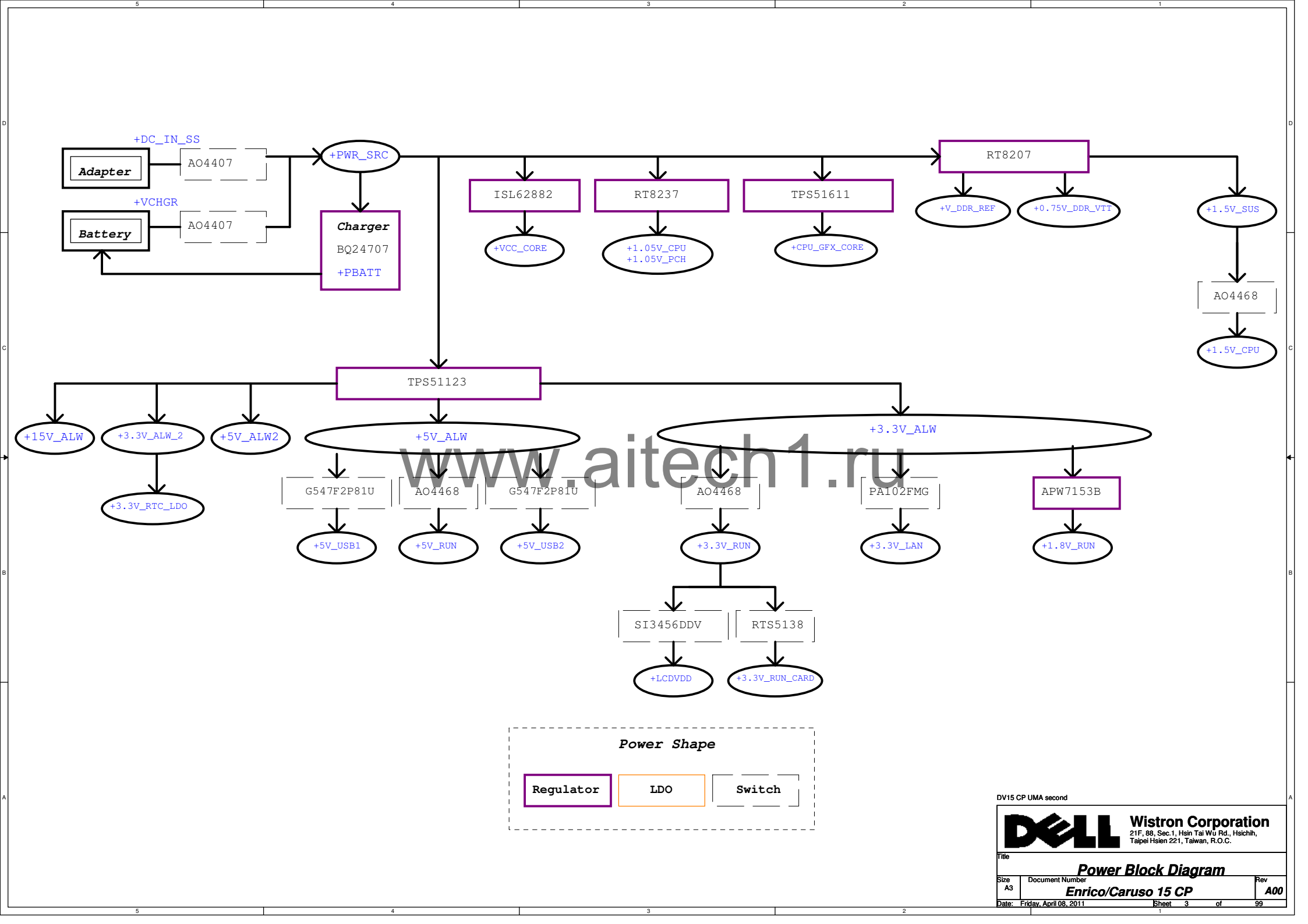
DV15 CP UMA second

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **Enrico/Caruso 15 CP** Rev: **A00**

Date: Friday, April 22, 2011 Sheet 2 of 99



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Power Block Diagram**

Size

Document Number

Rev

A3

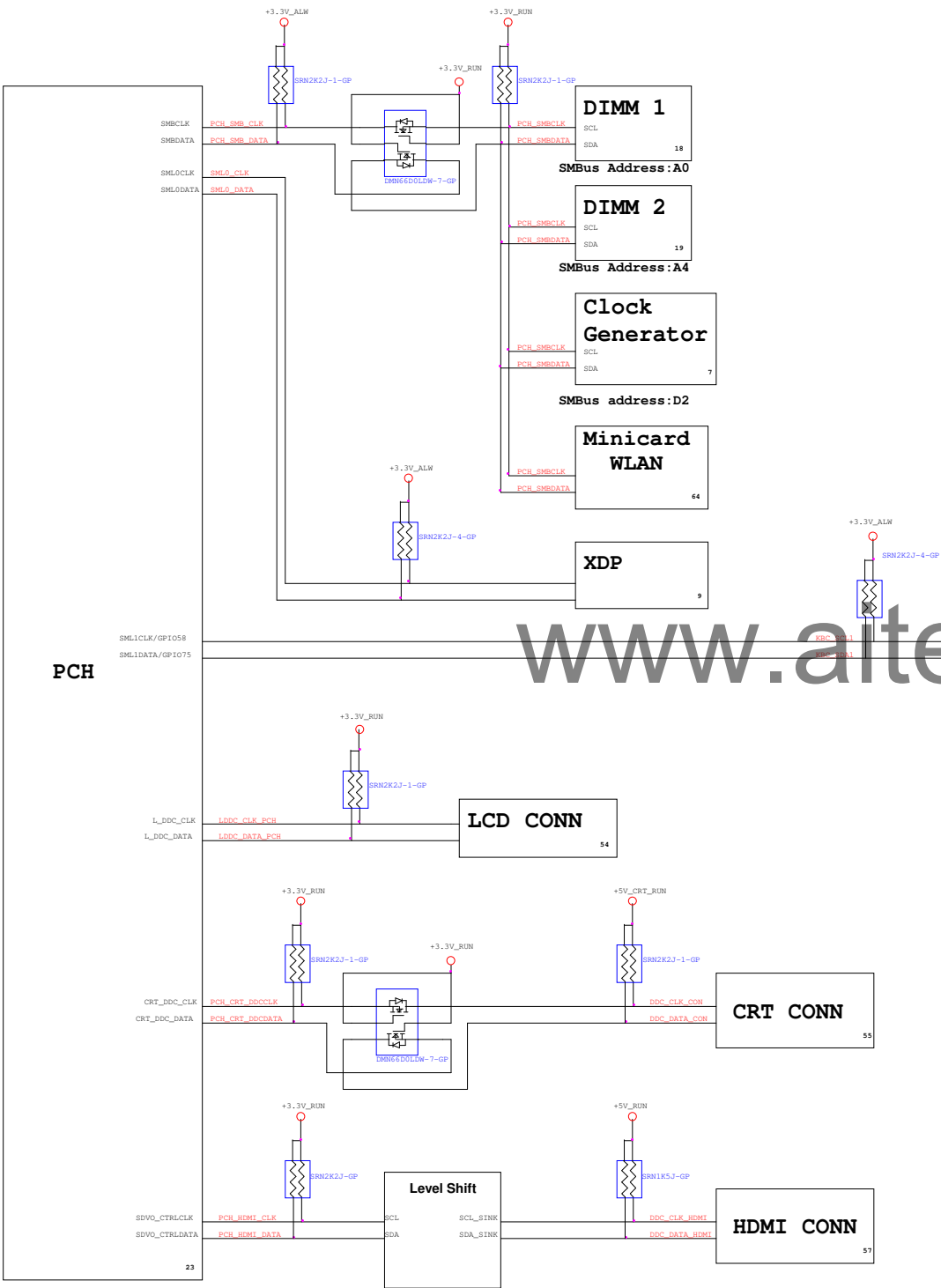
**Enrico/Caruso 15 CP**

A00

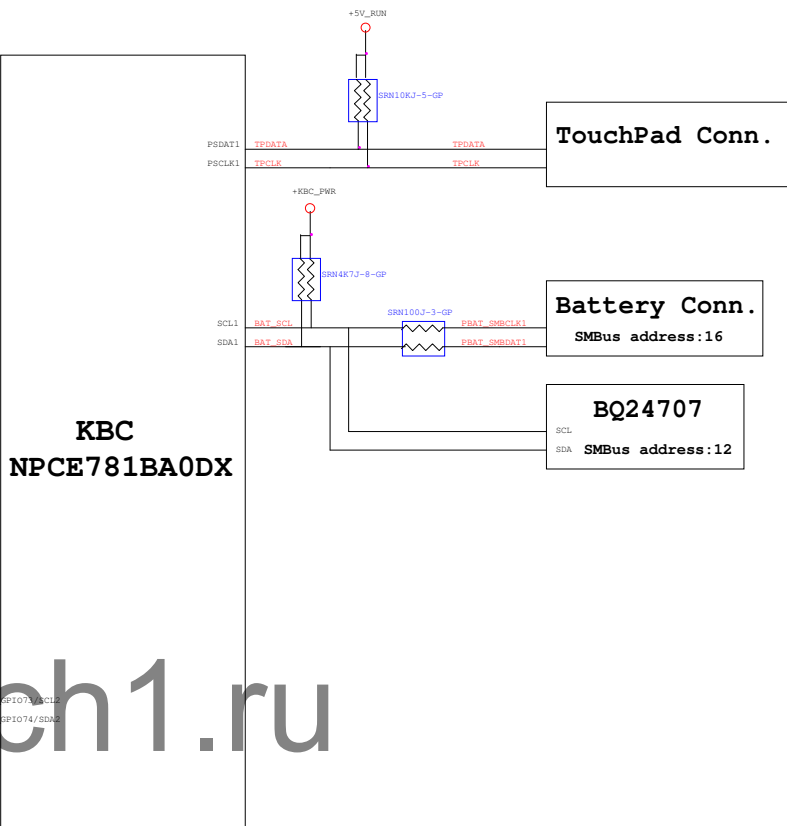
Date: Friday, April 08, 2011

Sheet 3 of 99

PCH SMBus Block Diagram



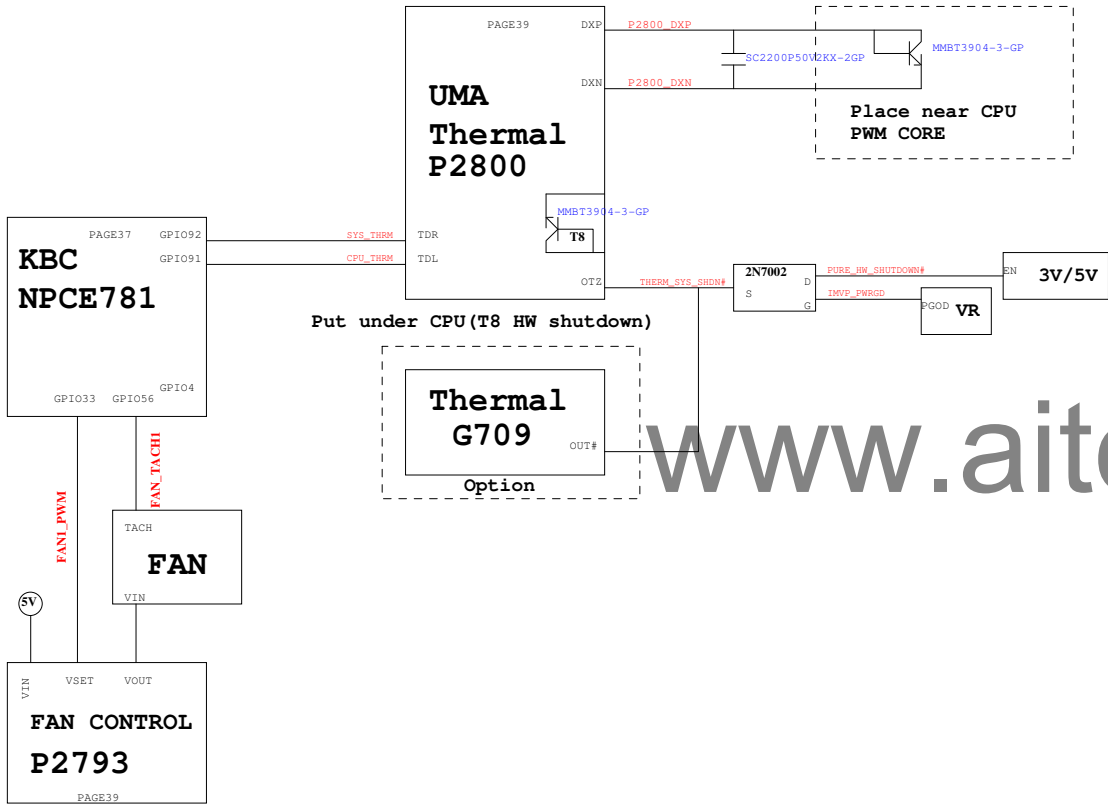
KBC SMBus Block Diagram



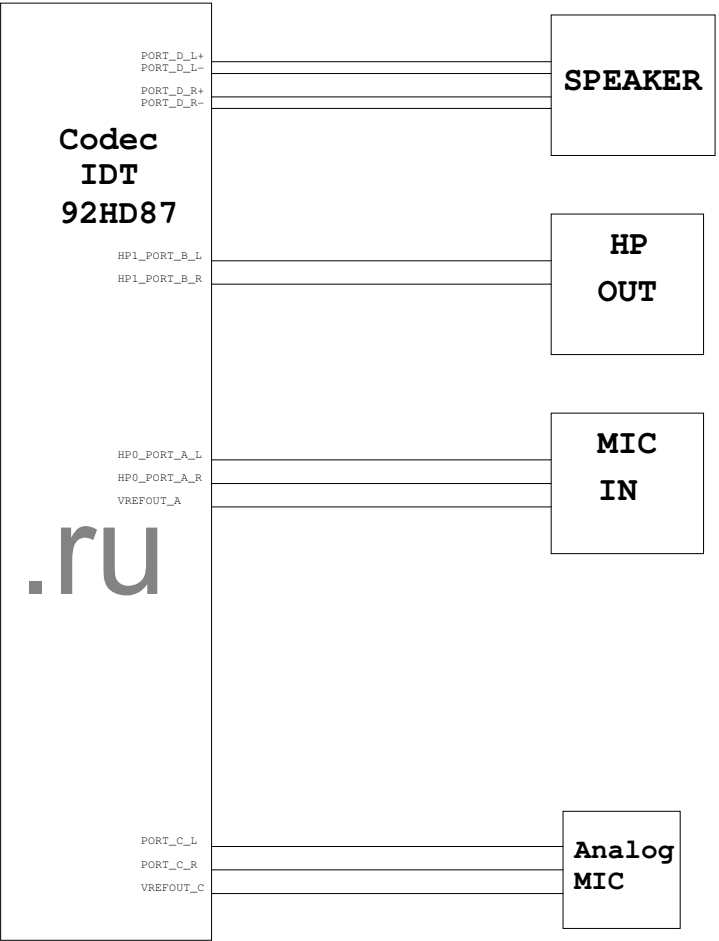
www.aitech1.ru



# Thermal Block Diagram



# Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#/GPIO51	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)</b> = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overriden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

## USB Table

USB	
Pair	Device
0	X
1	USB1
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

## Processor Strapping

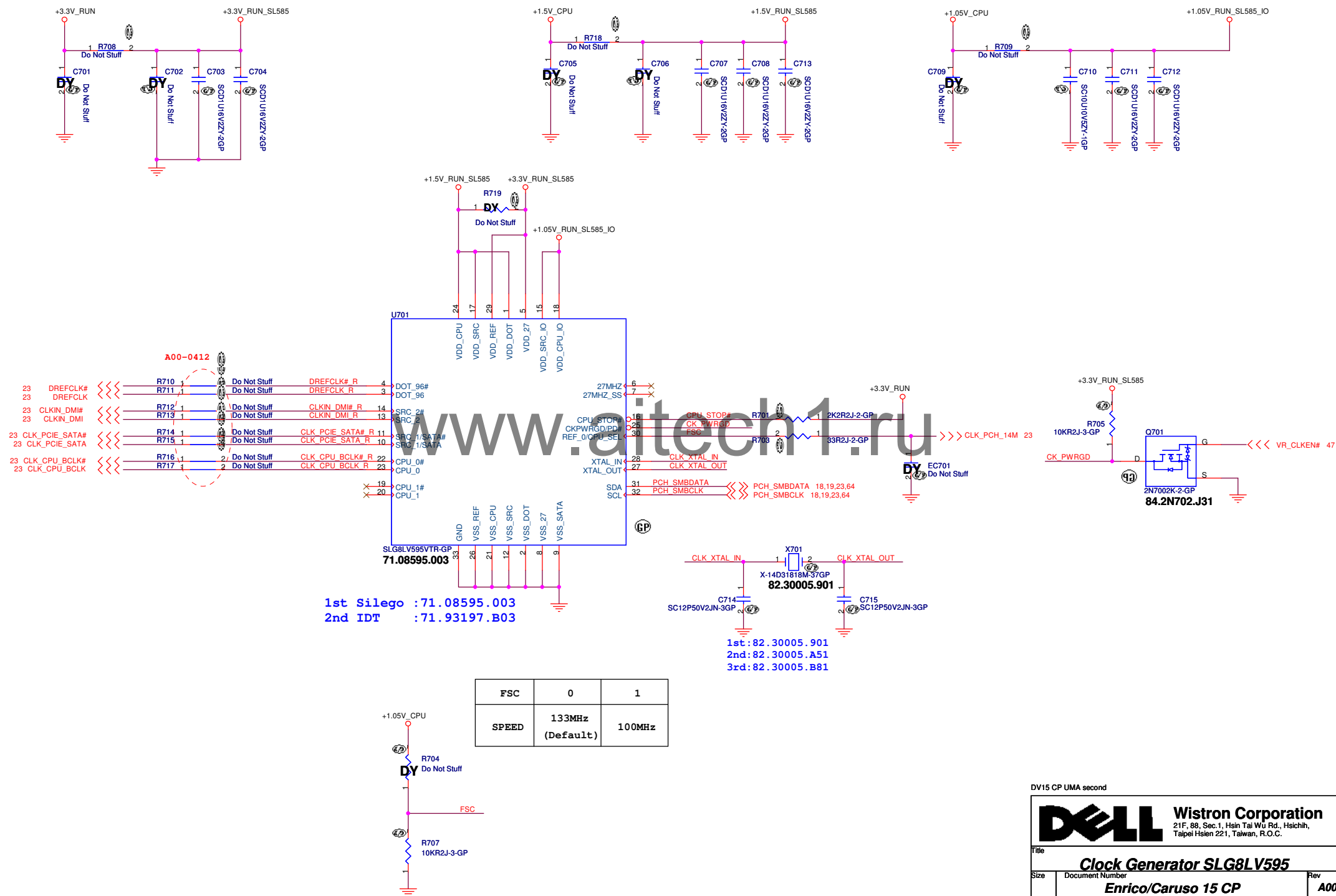
Calpella Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	<b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	<b>1:</b> Single PCI-Express Graphics <b>0:</b> Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1)</b> - Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

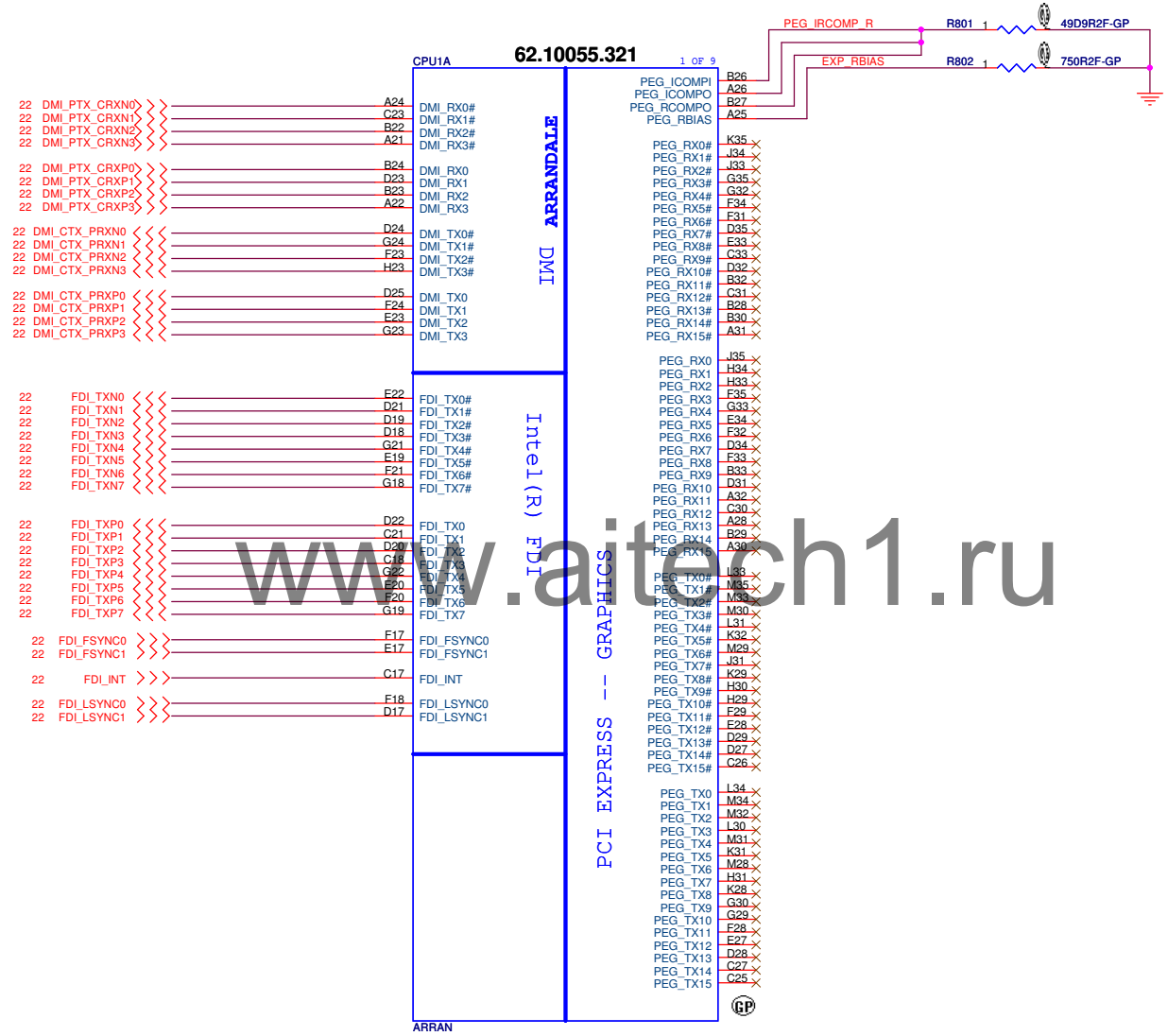
DV15 CP UMA second

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Table of Content</b>			
Size A3	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011	Sheet 6	of	99

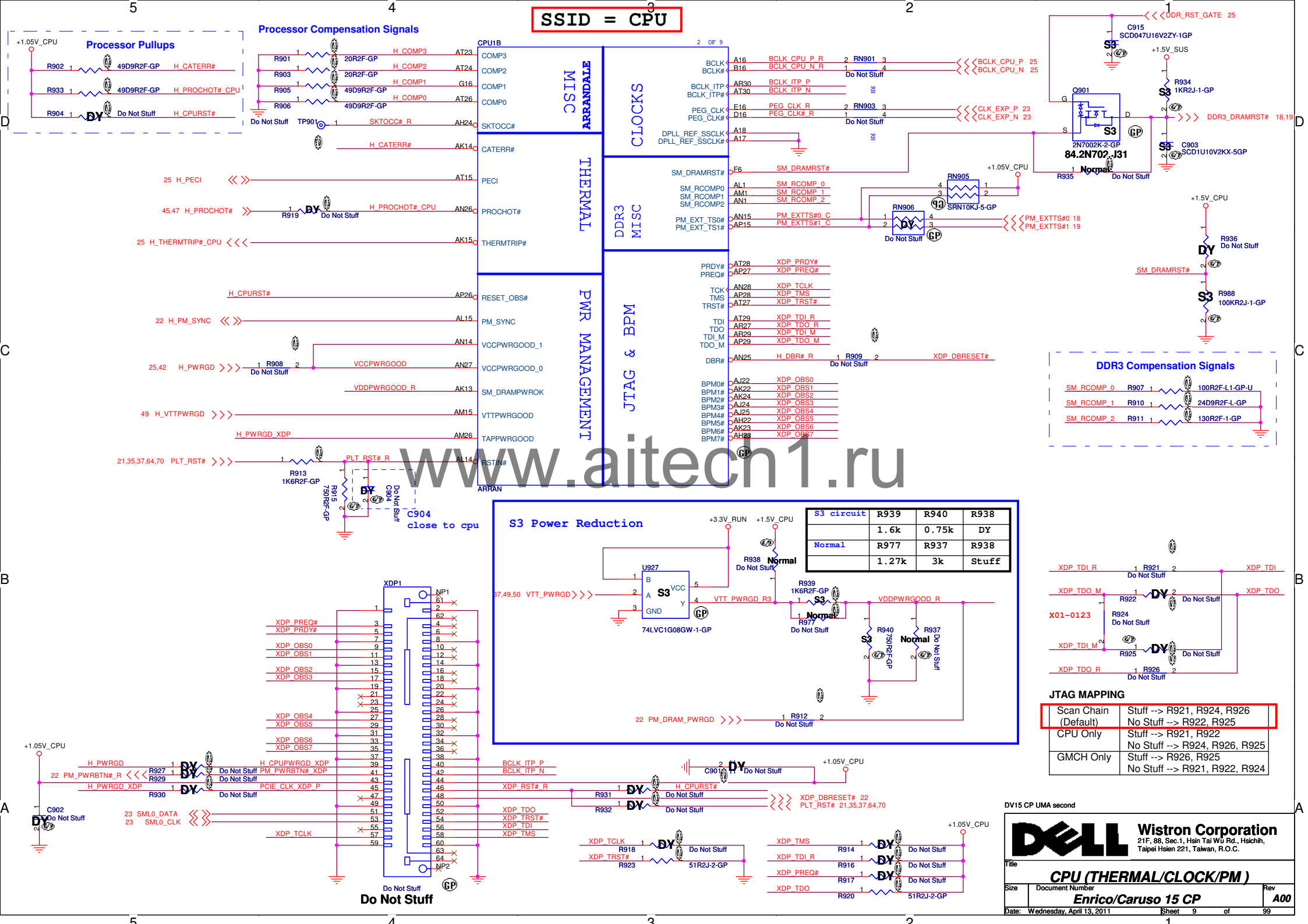
**SSID = CLOCK**



SSID = CPU



SSID = CPU



JTAG MAPPING		
Scan Chain (Default)	Stuff --> R921, R924, R926	
CPU Only	Stuff --> R921, R922	
GMCH Only	Stuff --> R926, R925	
	No Stuff --> R921, R922, R924	

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

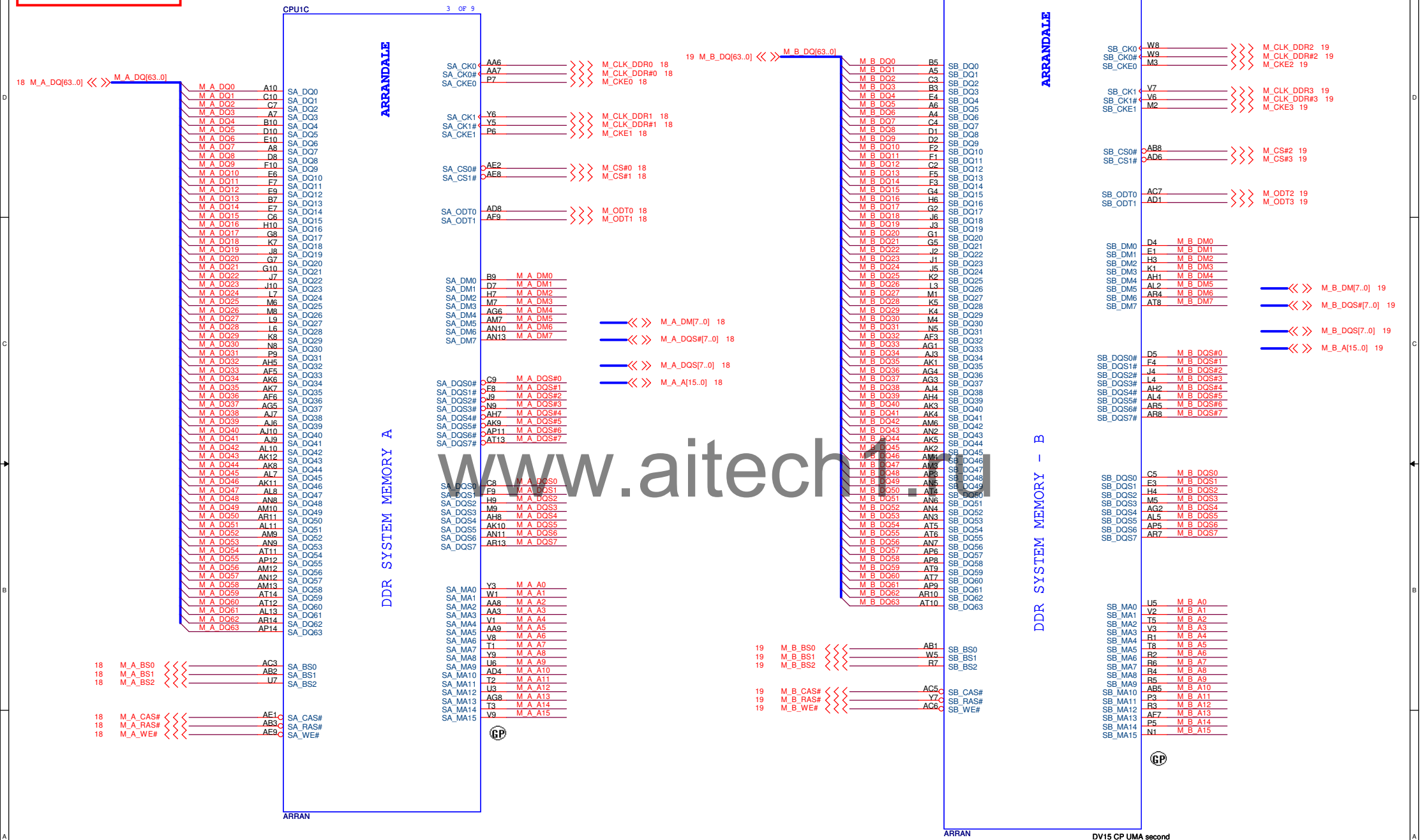
**DELL**

File  
**CPU (THERMAL/CLOCK/PM)**

Size Document Number  
**Enrico/Caruso 15 CP**

Date: Wednesday, April 13, 2011 Sheet 9 of 99

**SSID = CPU**



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (DDR)**

Size	Document Number
------	-----------------

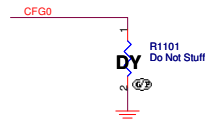
**Enrico/Caruso 15 CP**

Date: Wednesday, April 13, 2011

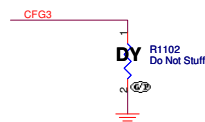
Sheet 10 of 99

Rev

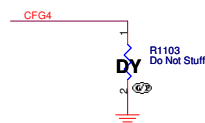
SSID = CPU



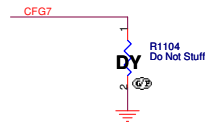
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



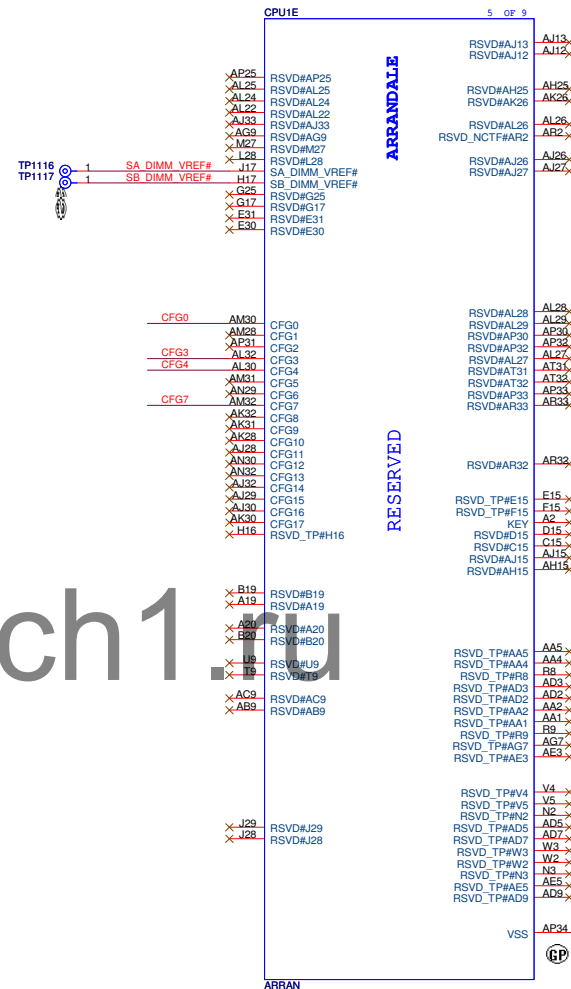
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

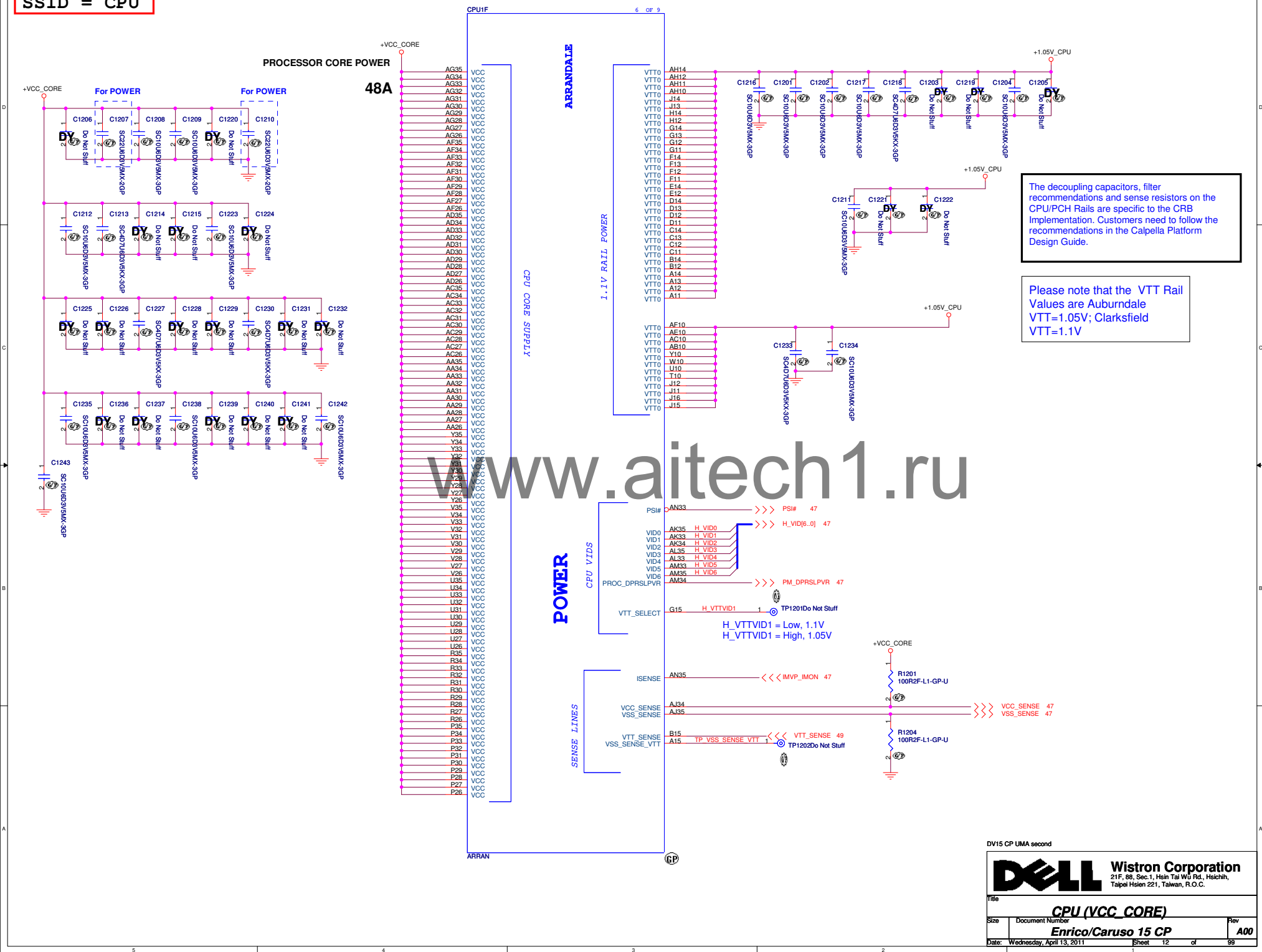


DV15 CP UMA second



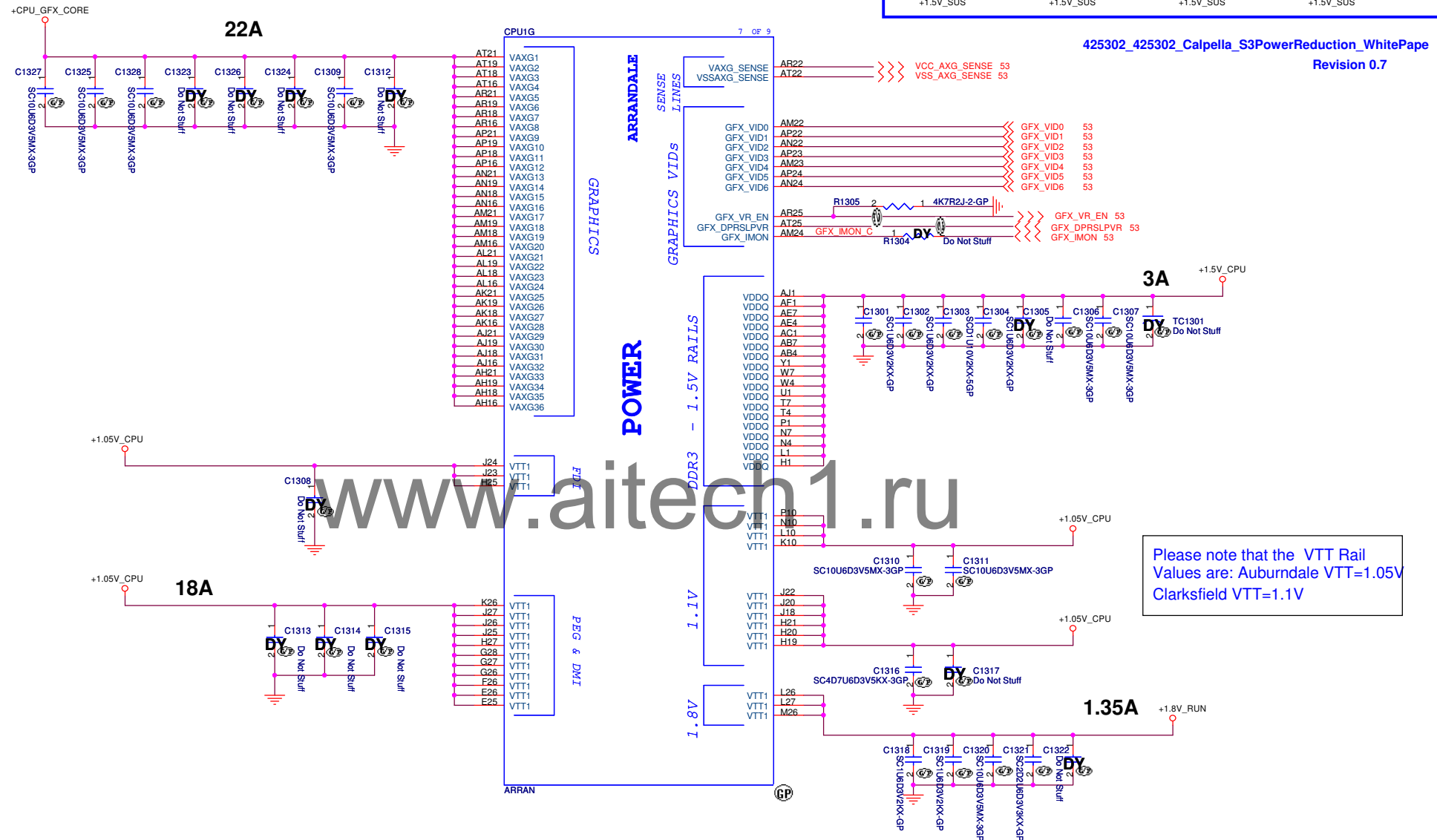
Title		
CPU (RESERVED)		
Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00
Date:	Friday, April 08, 2011	Sheet 11 of 99

**SSID = CPU**





**SSID = CPU**



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
...	...	...	...	...	...

**CPU (VCC GFXCORE)**

Size	Document Number
------	-----------------

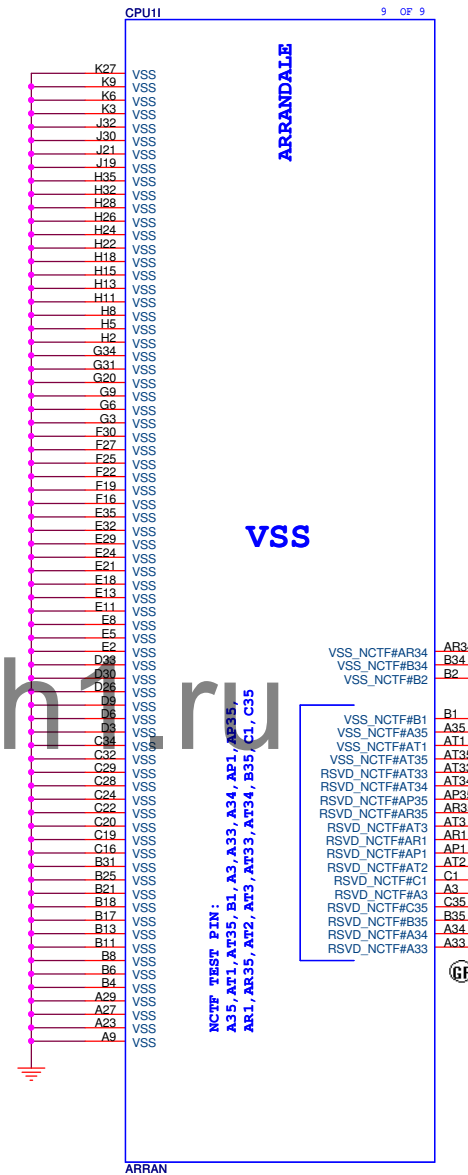
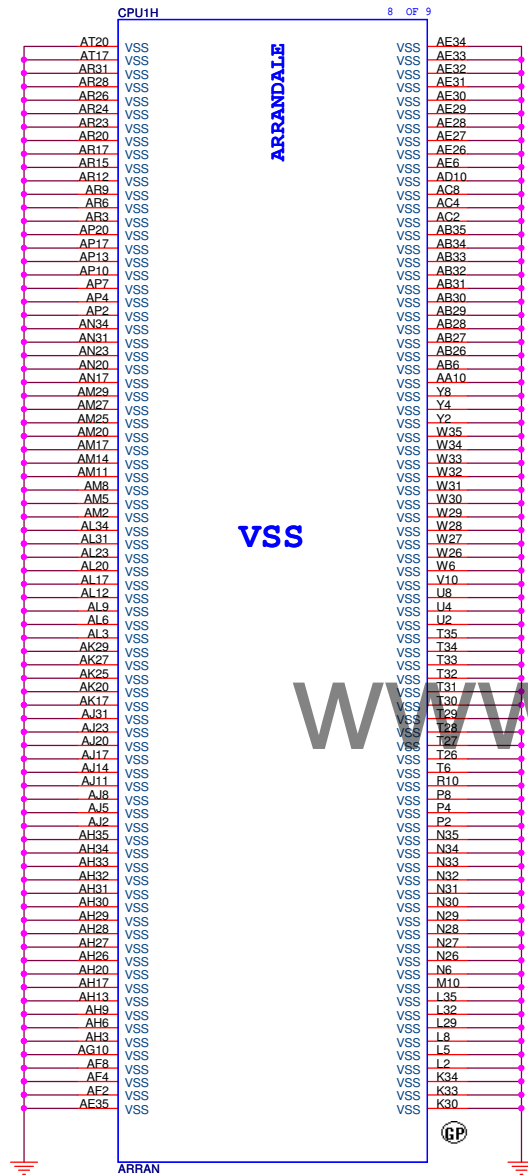
**Enrico/Caruso 15 CP**

Date: Wednesday, April 13, 2011

Sheet 13 of 99

**A00**

SSID = CPU



DV15 CP UMA second




**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title				
CPU (VSS)				
Size	Document Number			Rev
Enrico/Caruso 15 CP			A00	
Date:	Friday, April 08, 2011	Sheet	14	of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserved

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011		Sheet 15 of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
Enrico/Caruso 15 CP


Rev  
A00

Date: Friday, April 08, 2011Sheet 16 of 99

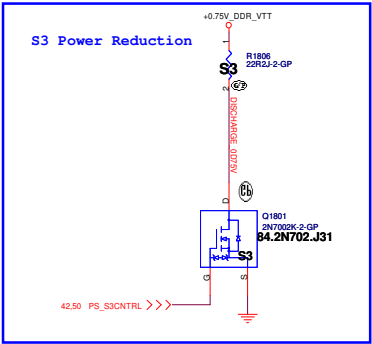
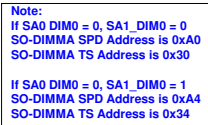
(Blanking)

www.aitech1.ru

DV15 CP UMA second

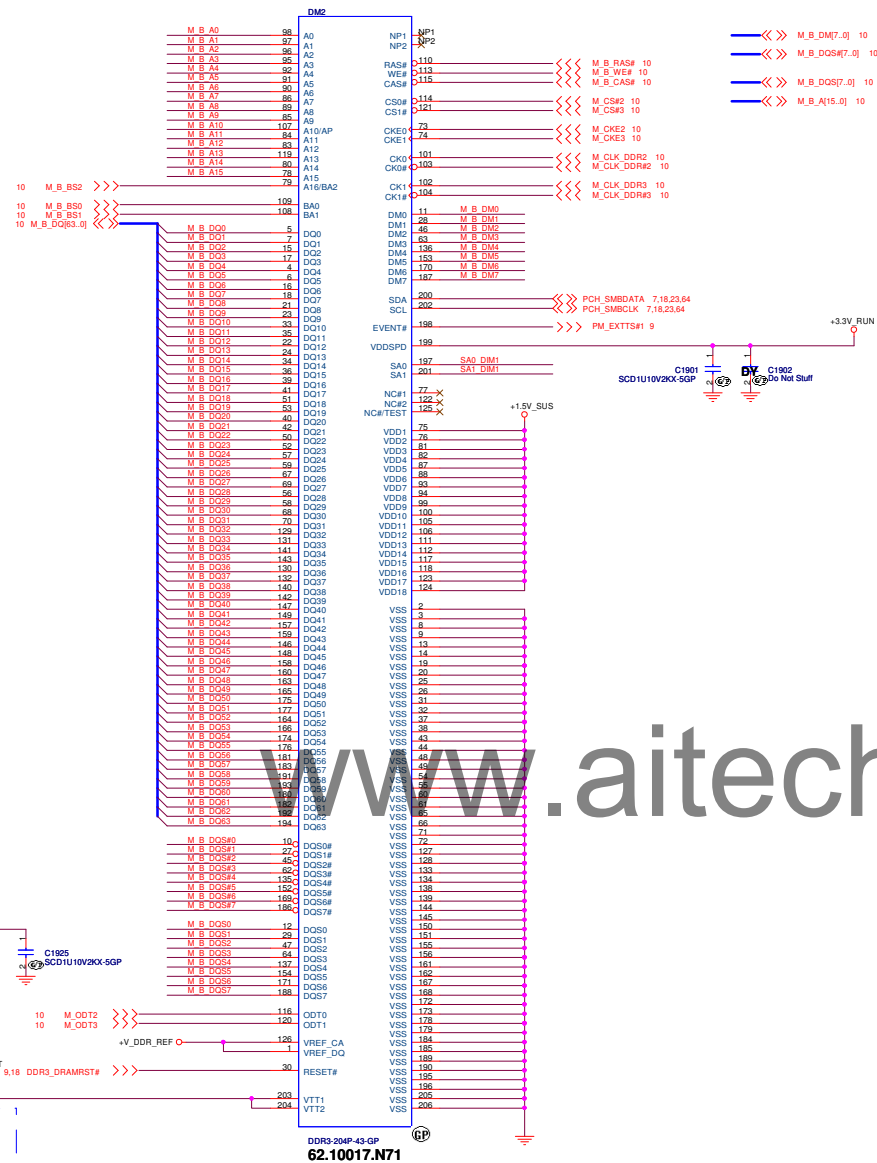
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A3	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011		Sheet 17	of 99

www.aitech.in



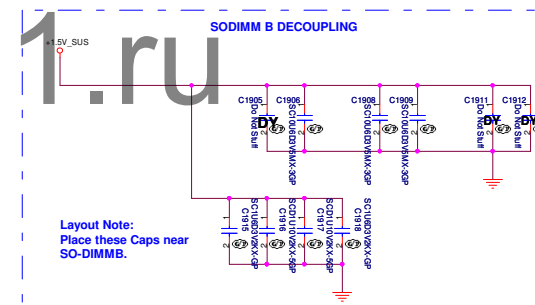
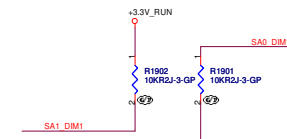
**62.10017.X31**

## SSID = MEMORY



**Note:**  
If SA0\_DIM1 = 0, SA1\_DIM1 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

If SA0\_DIM1 = 0, SA1\_DIM1 = 1  
SO-DIMMA SPD Address is 0xA4  
SO-DIMMA TS Address is 0x34



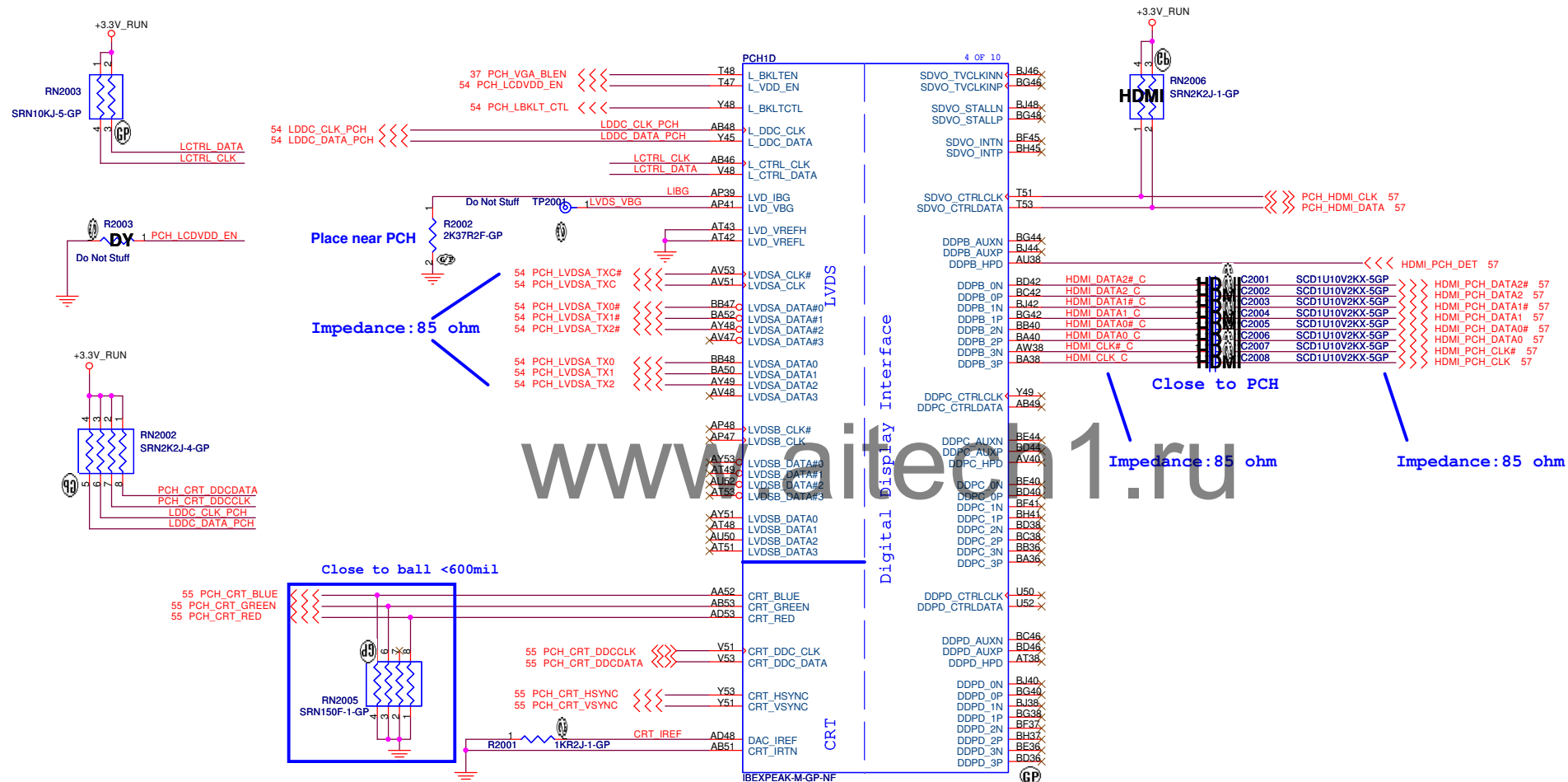
**Layout Note:**  
Place these 4  
SO-DIMMB.

Place these caps close to VTT1 and VTT2.

**Note:**  
SO-DIMMB SPD Address is 0xA  
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

**SSID = PCH**



DV15 CP UMA second

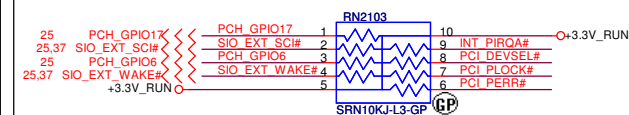
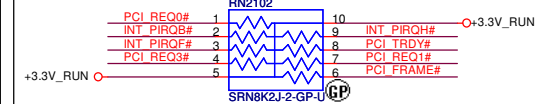
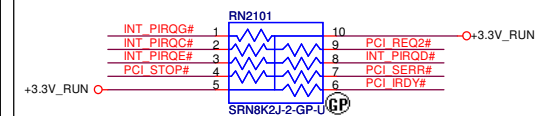


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>PCH (LVDS/CRT/DDI)</b>			
Size	Document Number	Rev	
	<b>Enrico/Caruso 15 CP</b>		<b>A00</b>
Date:	Wednesday, April 13, 2011	Sheet	20 of 99



**SSID = PCH**

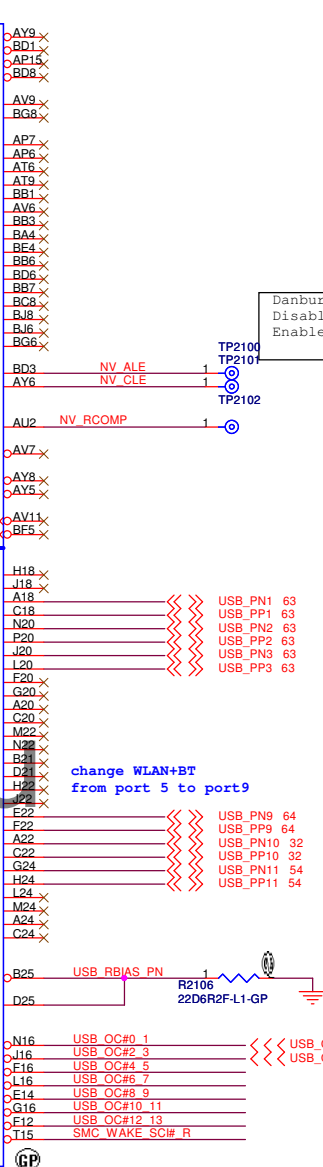
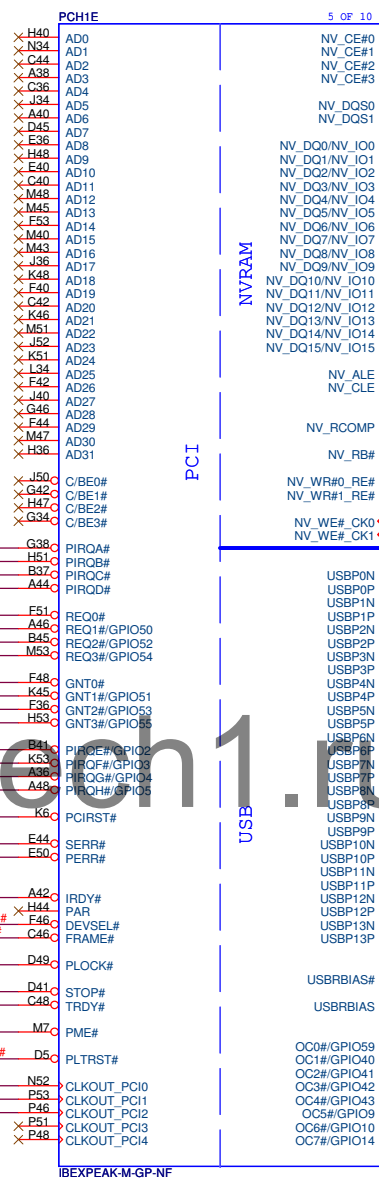
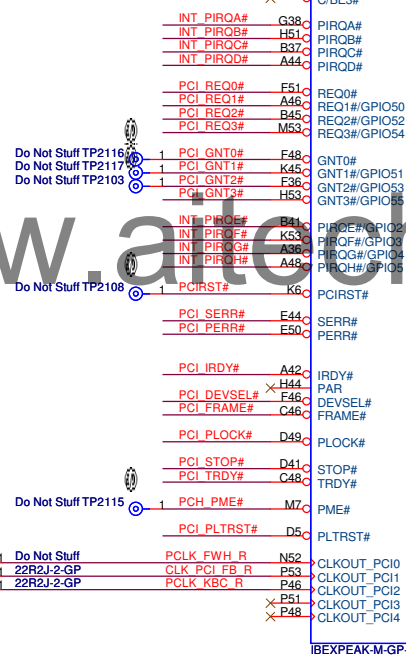
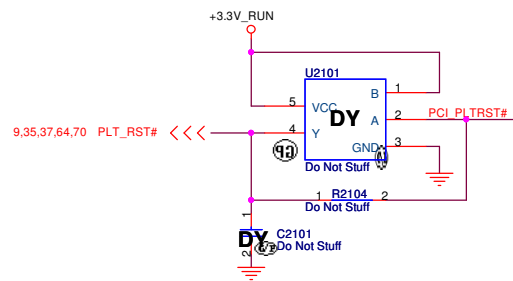
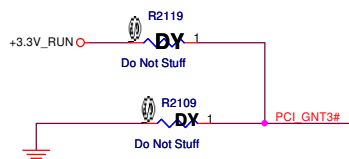


BOOT BIOS Strap

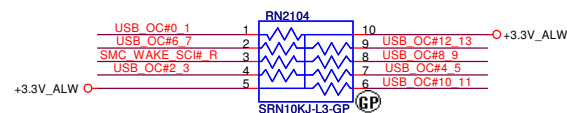
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block  
Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---



USB	
Pair	Device
0	X
1	USB1 (Debug Port)
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**PCH (PCI/USB/NVRAM)**

Size	Document Number
------	-----------------

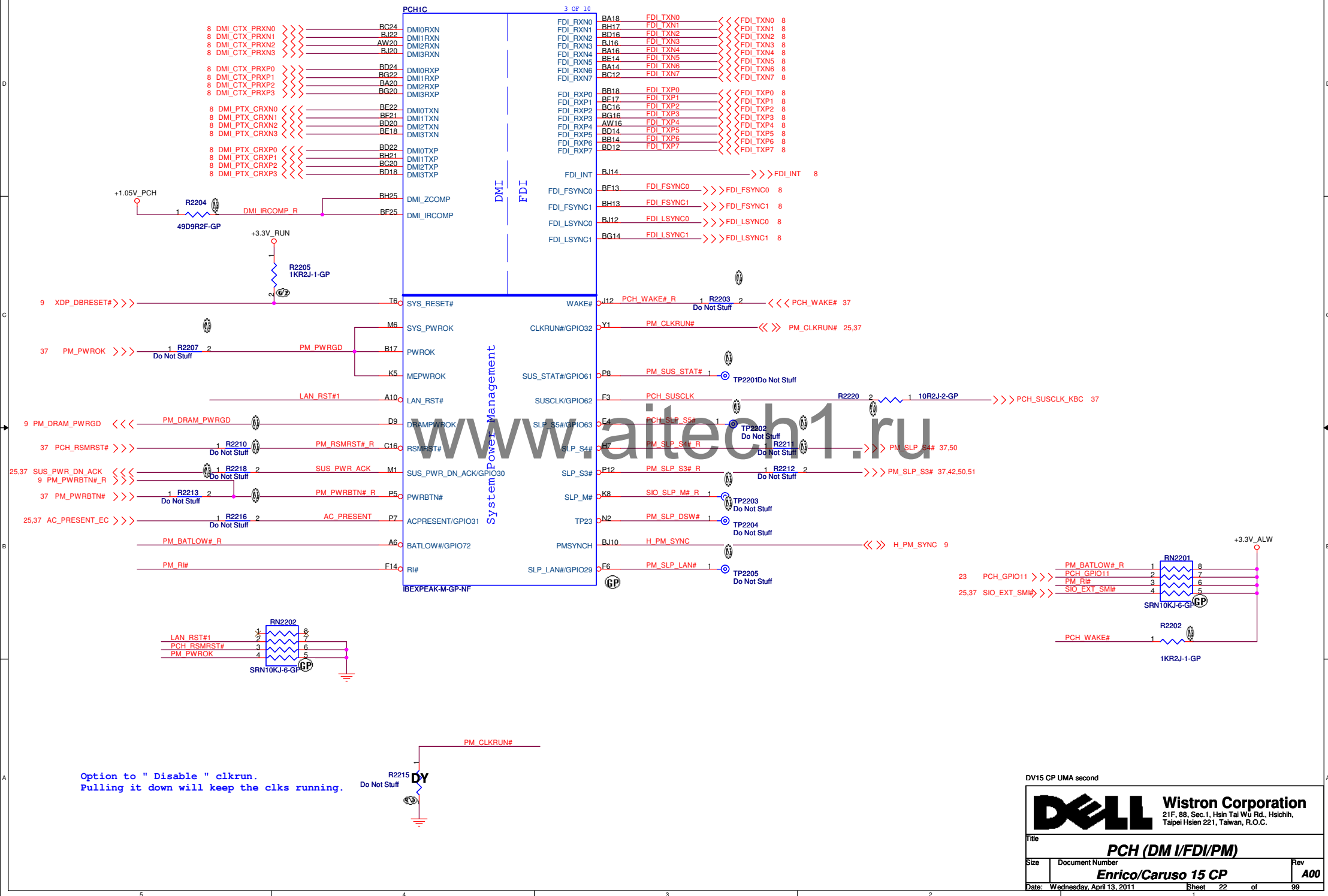
**Enrico/Caruso 15 CP**

Rev	
-----	--

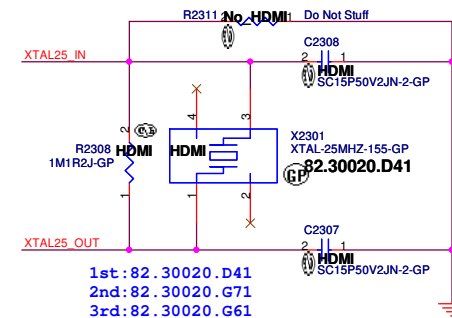
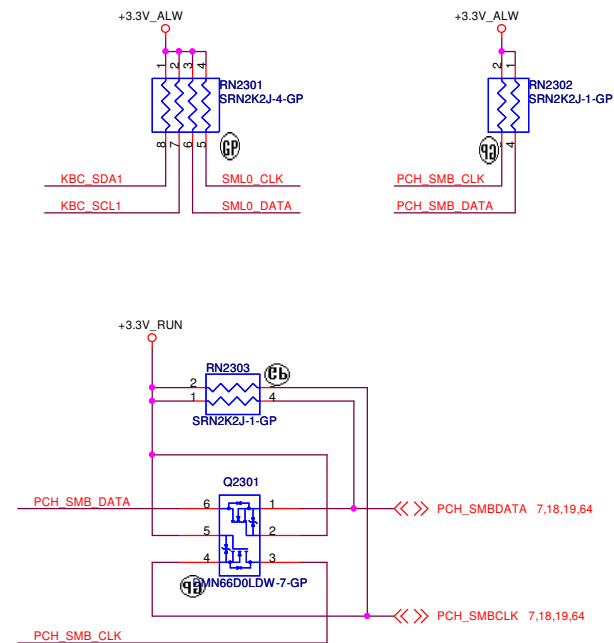
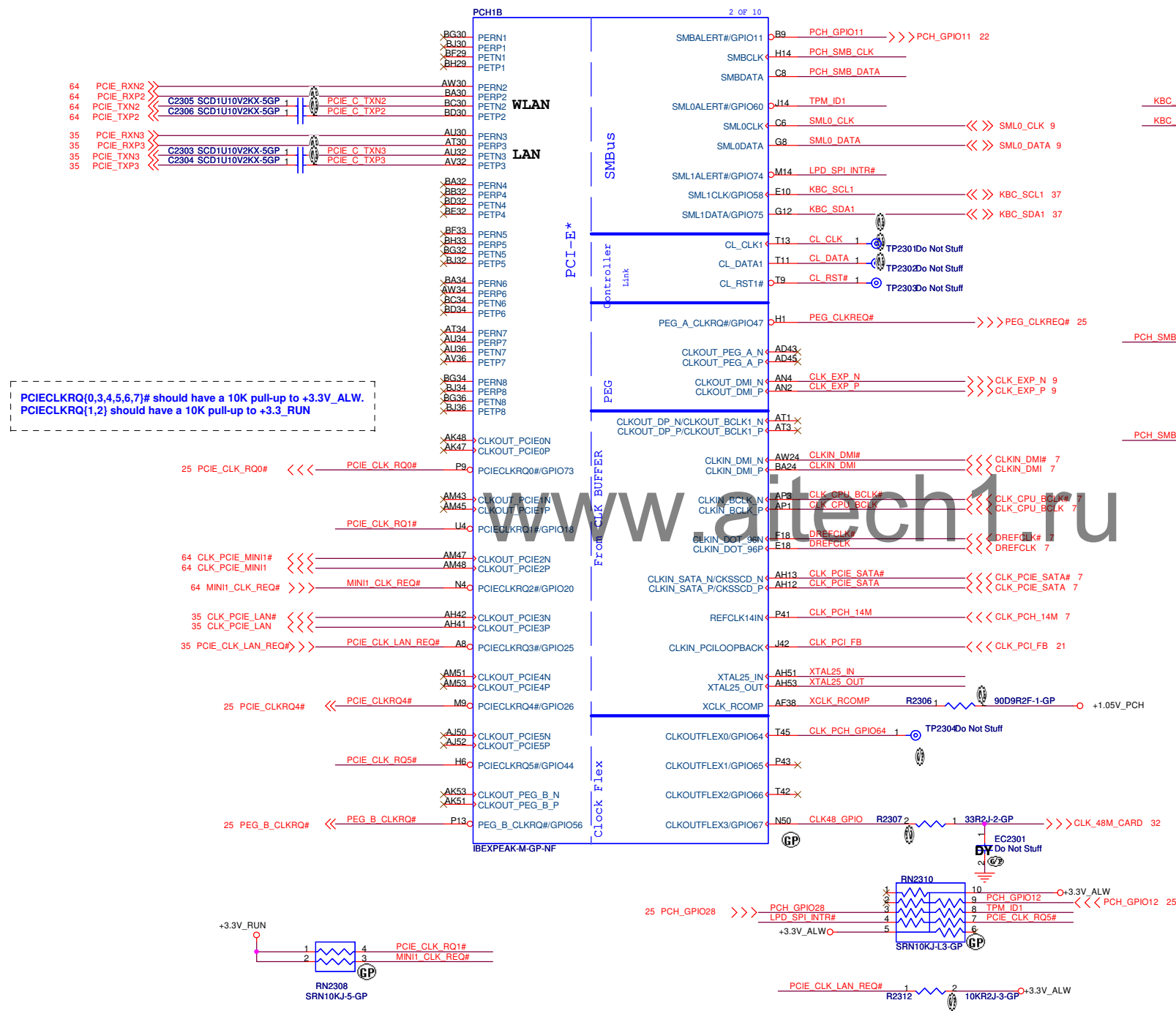
Date: Wednesday, April 13, 2011

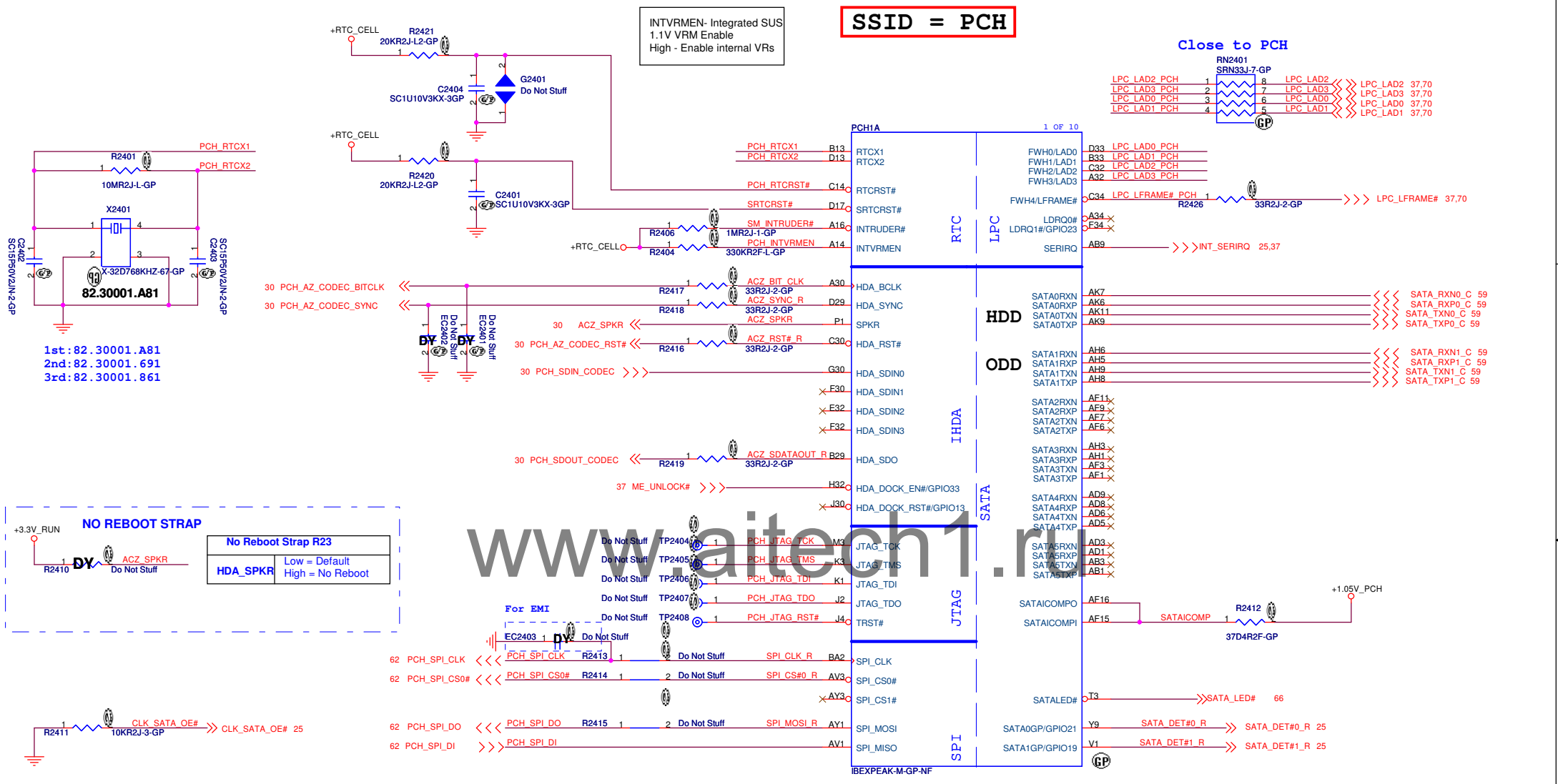
Sheet 21 of 99

SSID = PCH

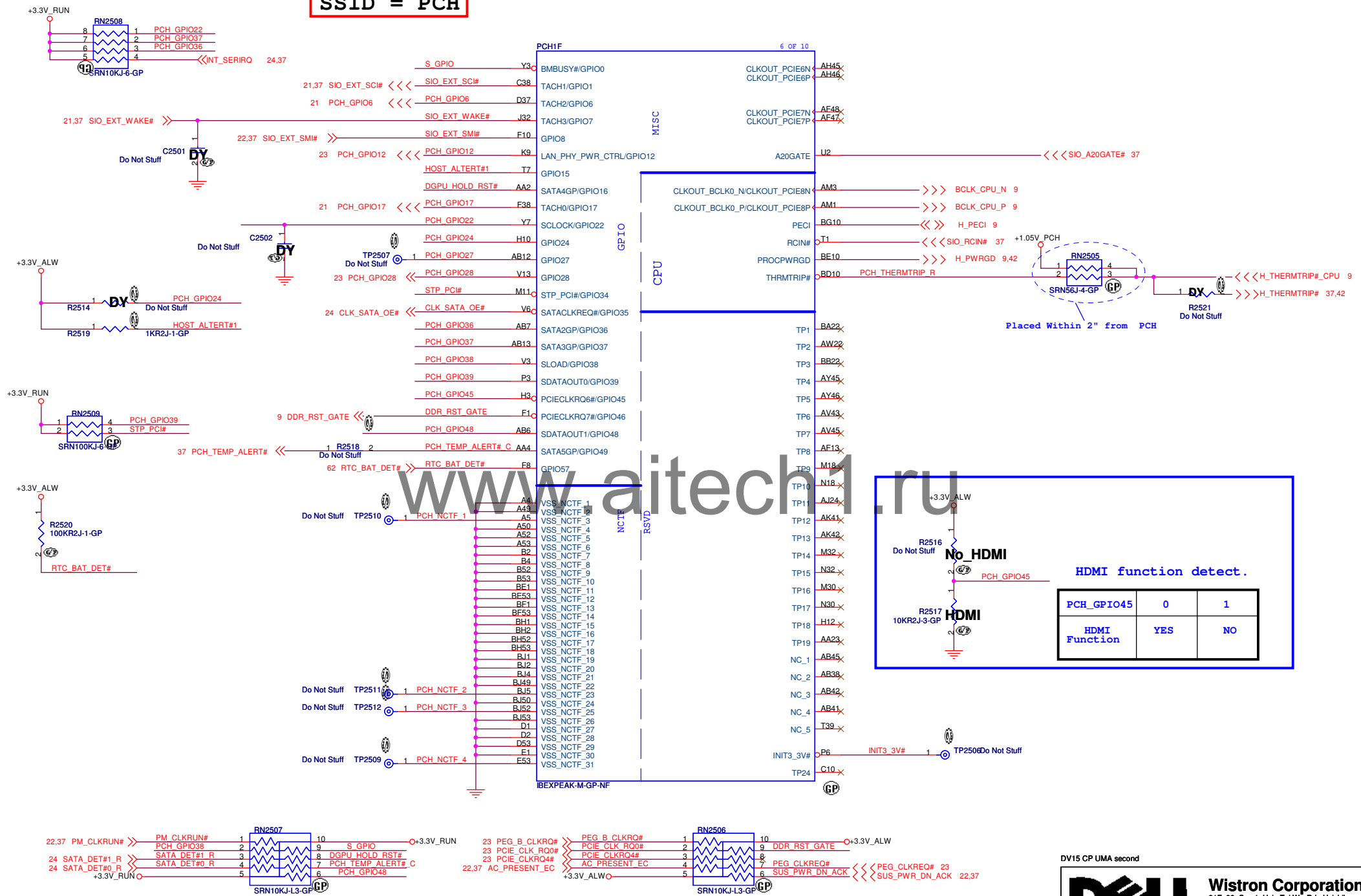


**SSID = PCH**



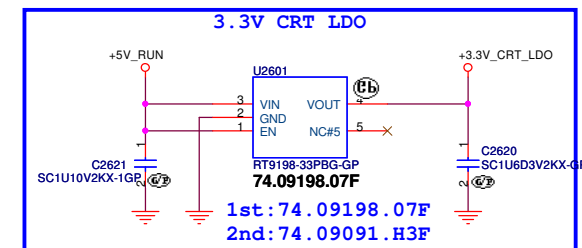
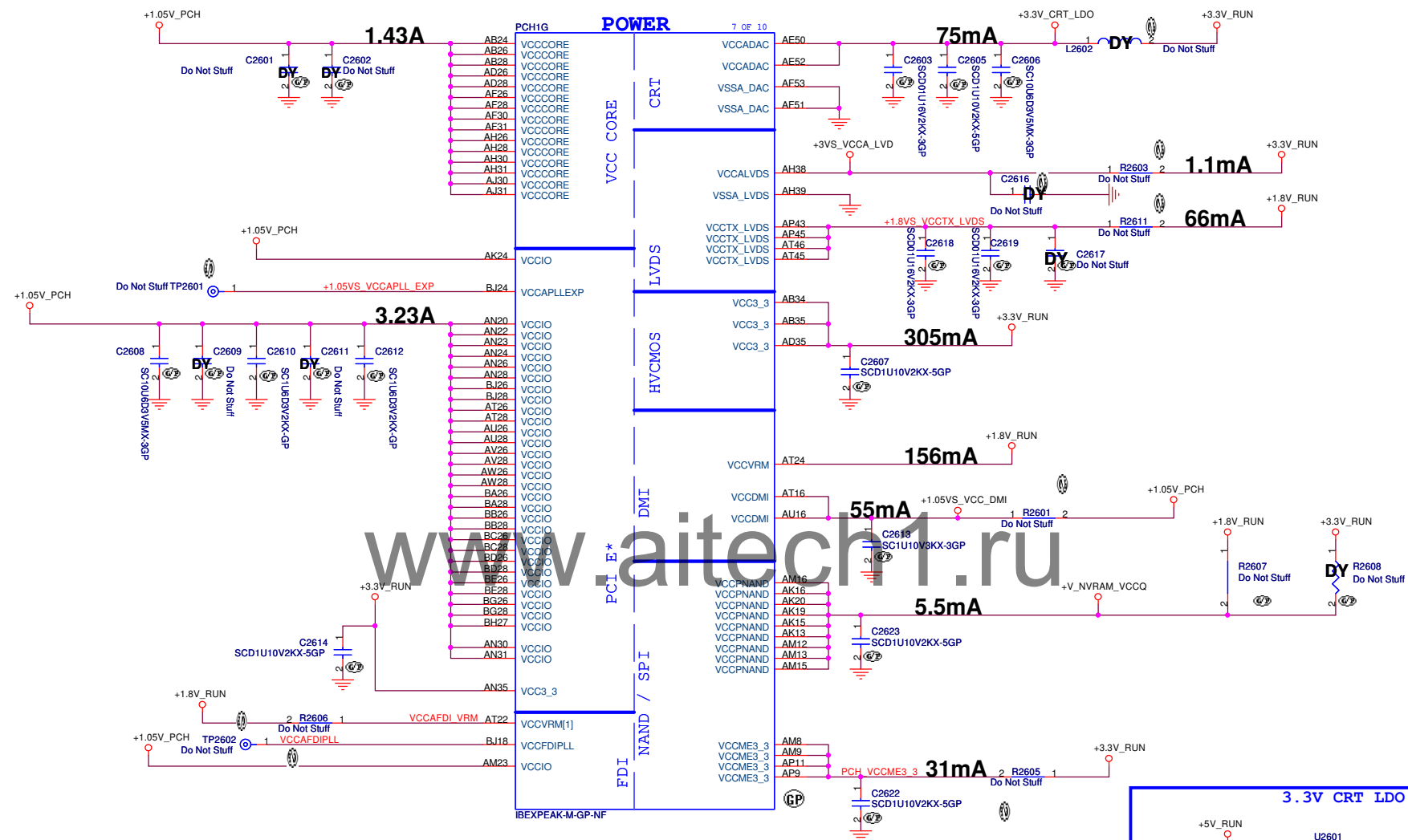


SSID = PCH



DV15 CP UMA second

**SSID = PCH**



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**PCH (POWER1)**

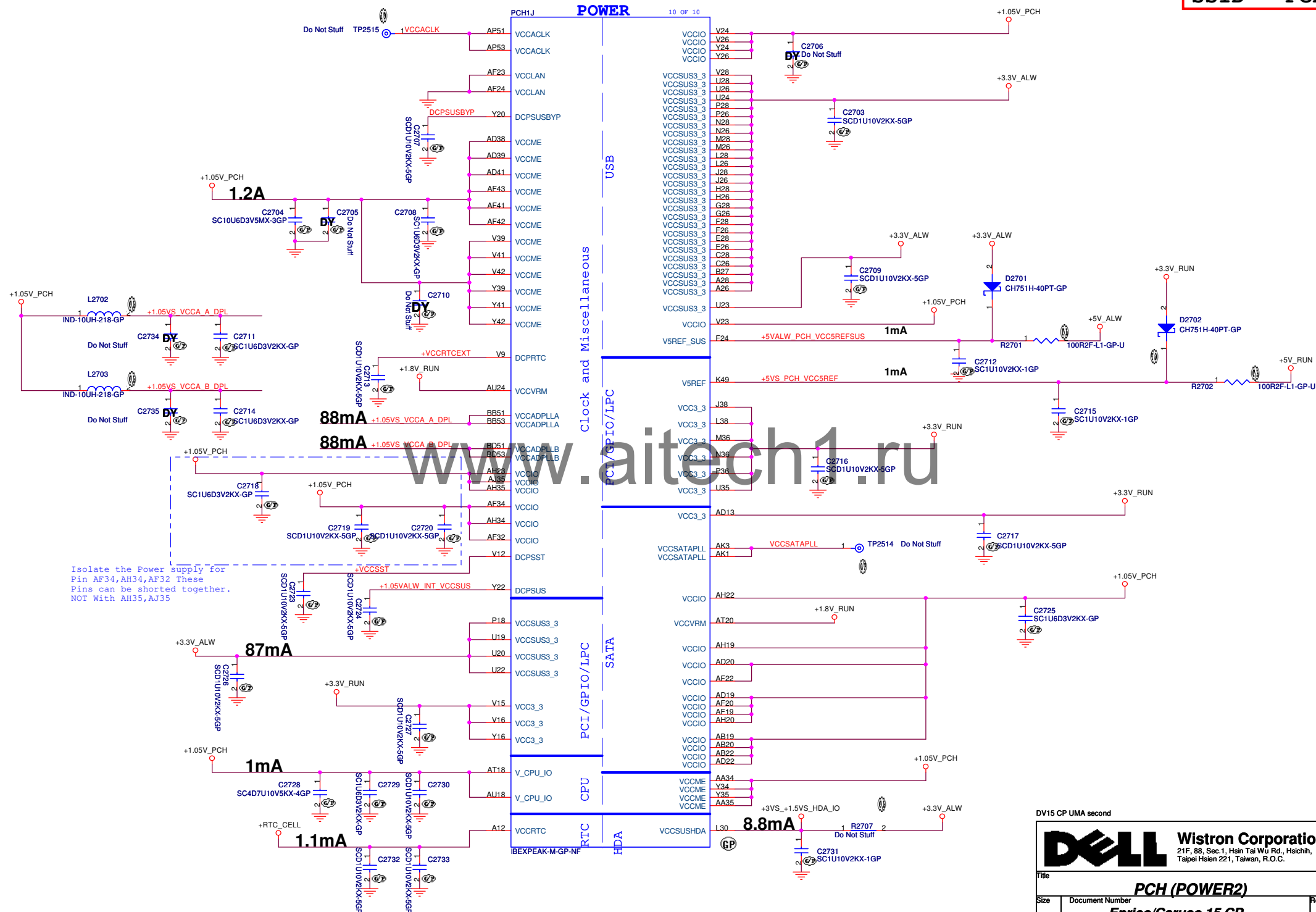
Size	Document Number
------	-----------------

**Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

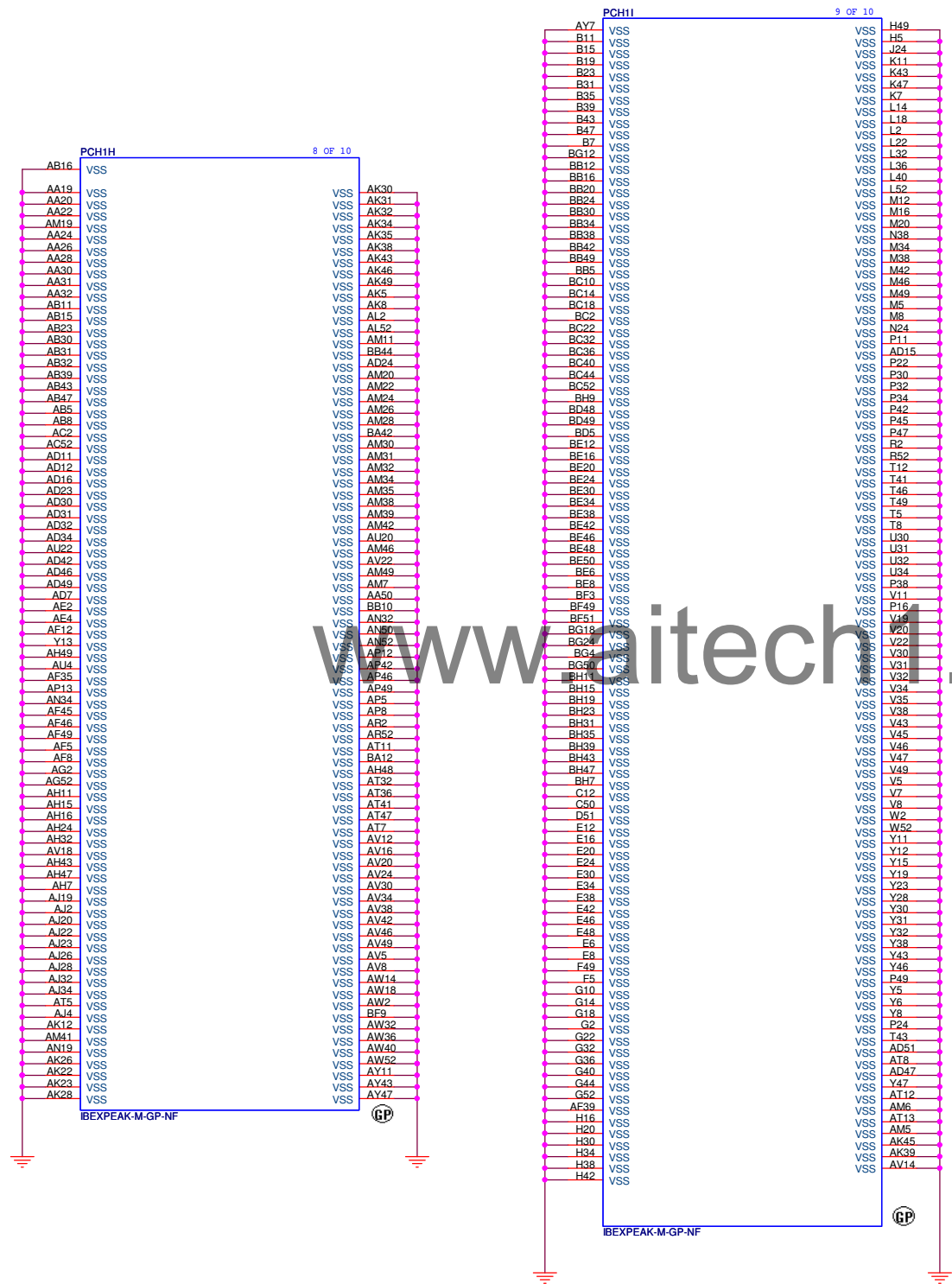
Sheet 26 of 99

Rev	<b>A00</b>
-----	------------





SSID = PCH






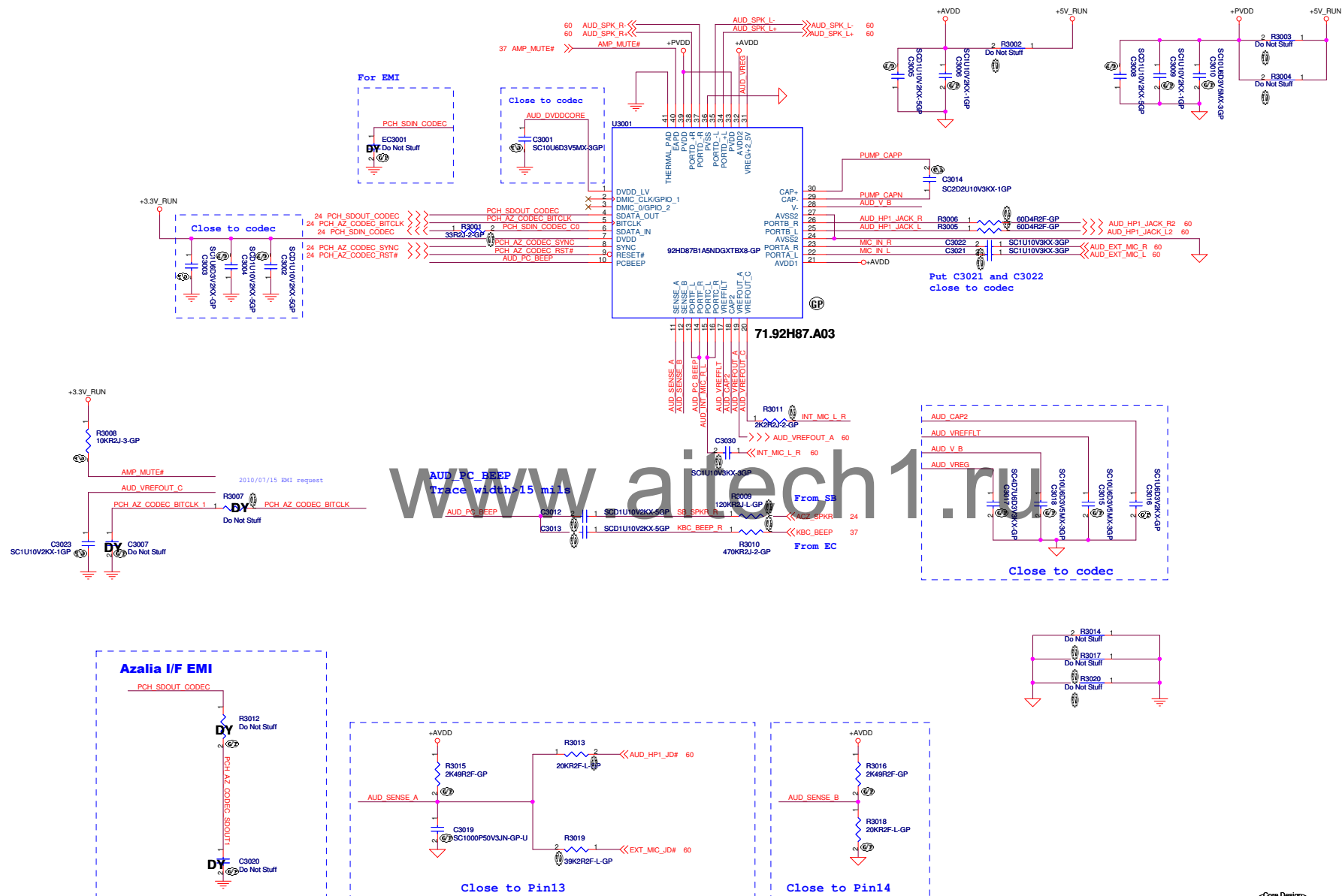
(Blanking)

www.aitech1.ru

DV15 CP UMA second

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A3	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011	Sheet	29	of 99


SSID = AUDIO



(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

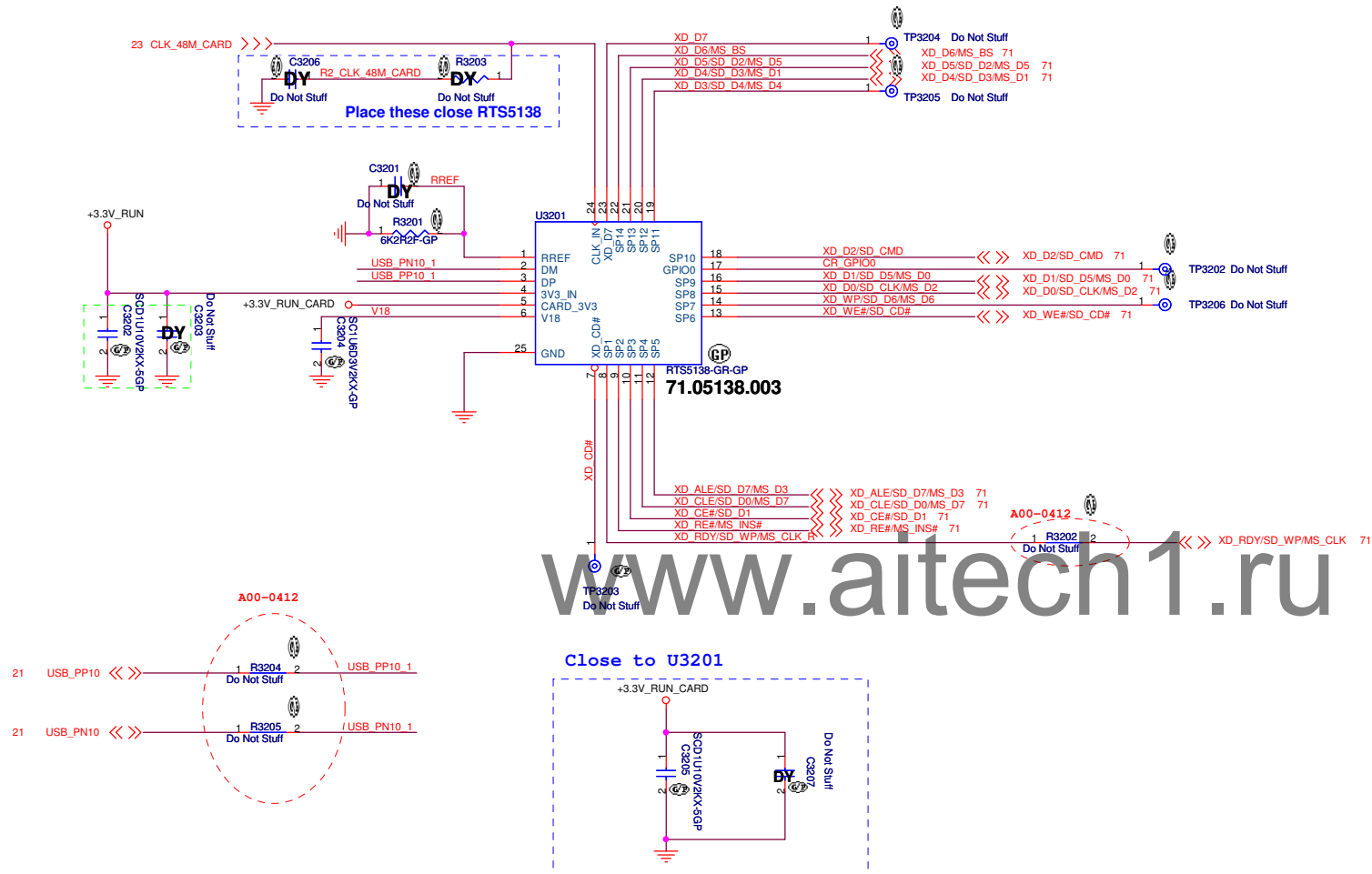
Size  
A3

Document Number  
Enrico/Caruso 15 CP

Rev  
A00

Date: Friday, April 08, 2011Sheet 31 of 99

SSID = SDIO



DV15 CP UMA second

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Card Reader-RTS5138</b>			
Size	Document Number	Rev	
Custom	<b>Enrico/Caruso 15 CP</b>		<b>A00</b>
Date:	Wednesday, April 13, 2011	Sheet	32 of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
Enrico/Caruso 15 CP


Rev  
A00

Date: Friday, April 08, 2011Sheet 33 of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

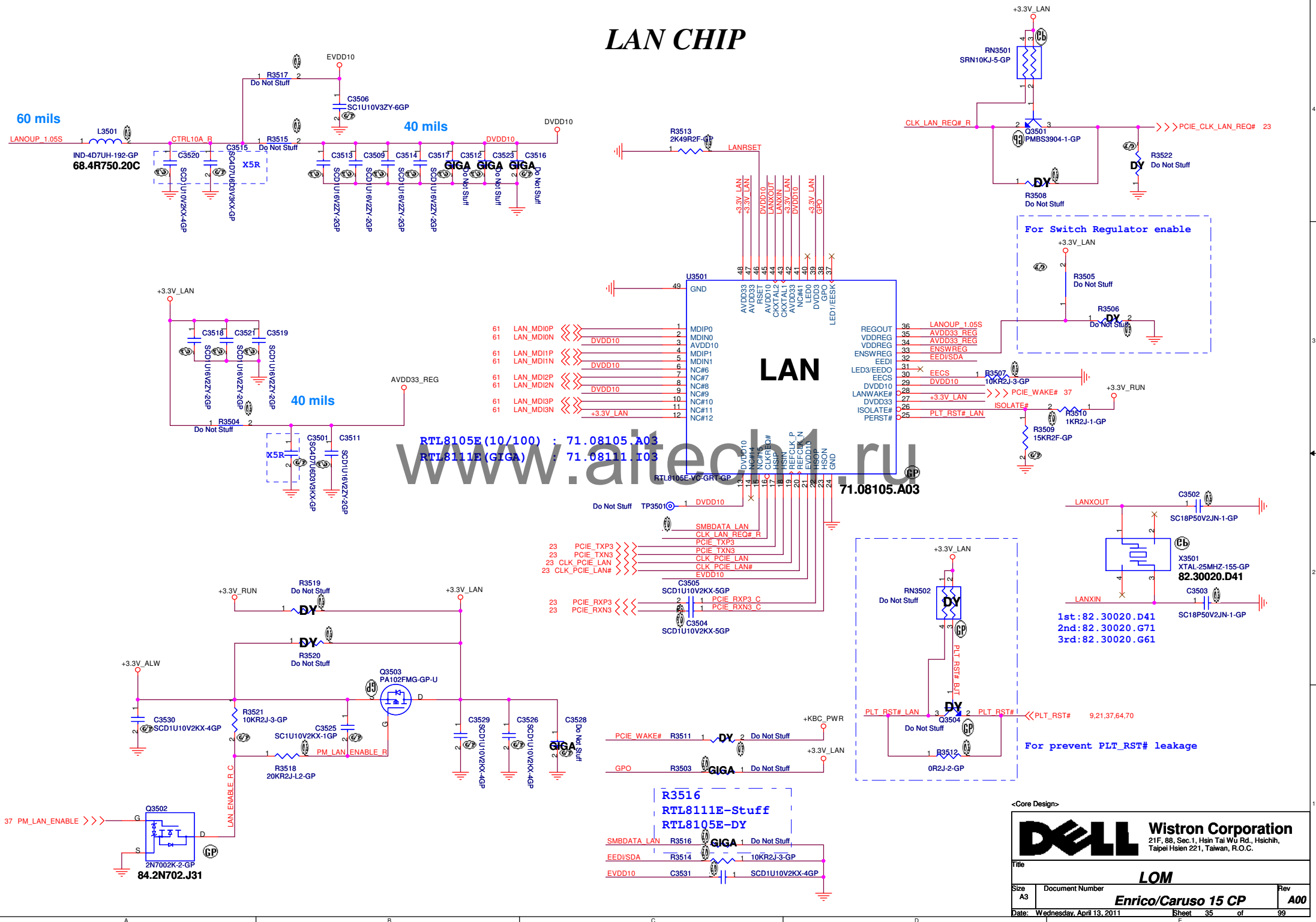
Document Number  
**Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

Rev  
**A00**

Sheet 34 of 99

# LAN CHIP



(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

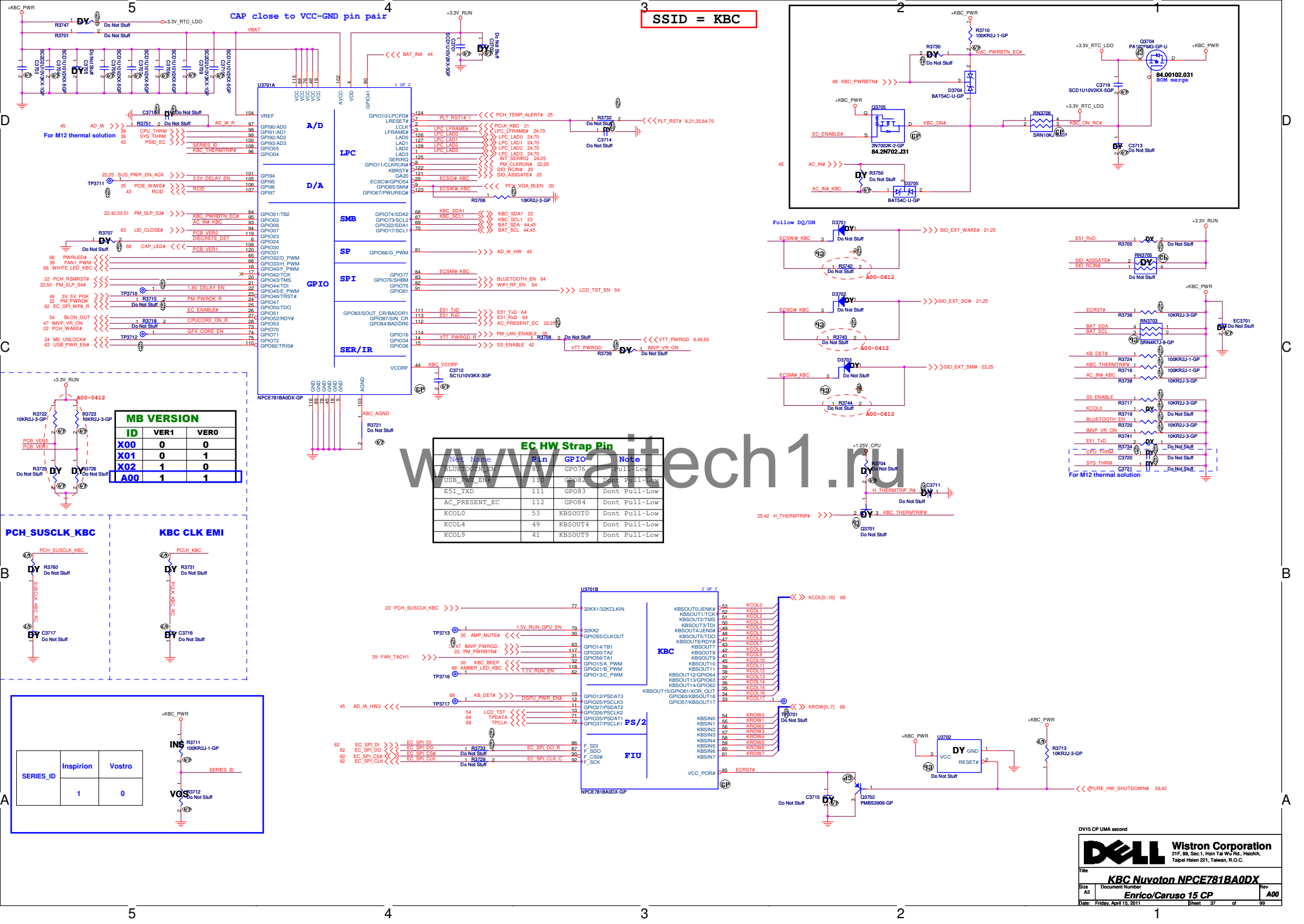
Document Number  
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Rev  
A00

Sheet 36 of 99






(Blanking)

www.aitech1.ru

DV15 CP UMA second



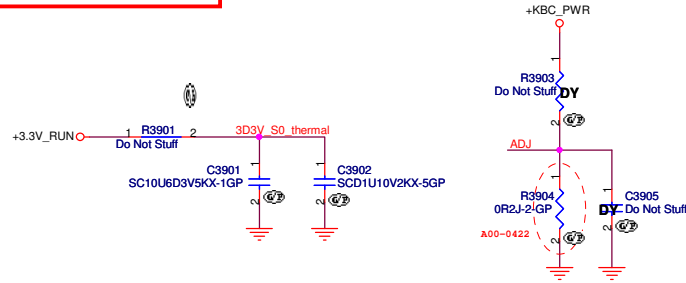
Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 38 of 99	

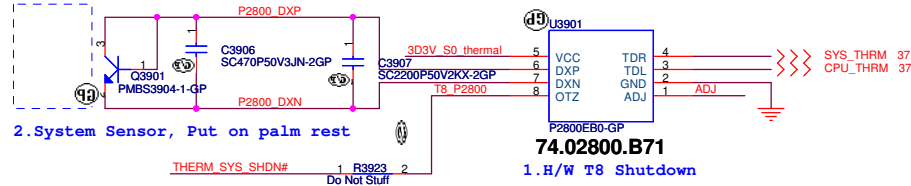
SSID = Thermal



Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.

## Thermal sensor P2800

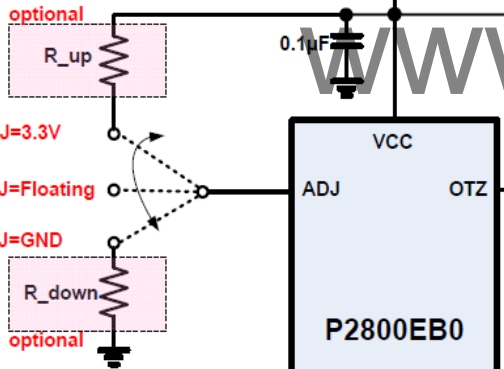
Remove R3908 and  
put C3906 close to Q3901



2. System Sensor, Put on palm rest

THERM\_SYS\_SHDN#

3.0V to 3.6V

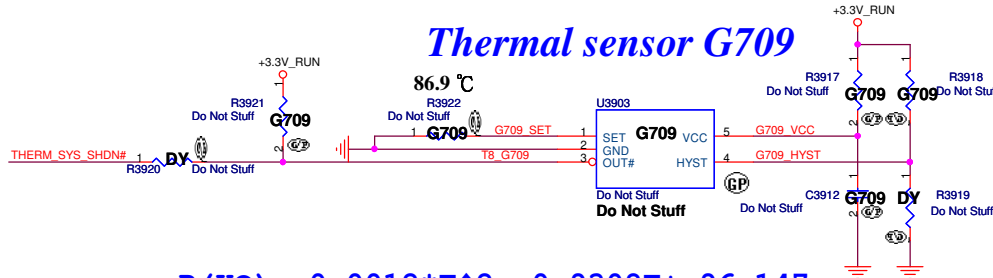


Option 1: OTZ=95°C → ADJ=3.3V

Option 2: OTZ=85°C → ADJ=Floating

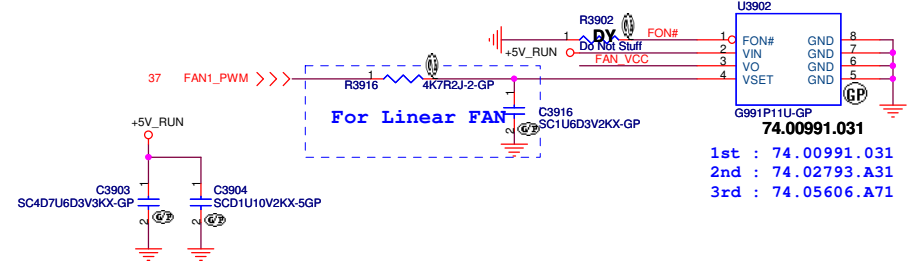
Option 3: OTZ=90°C → ADJ=GND

## Thermal sensor G709



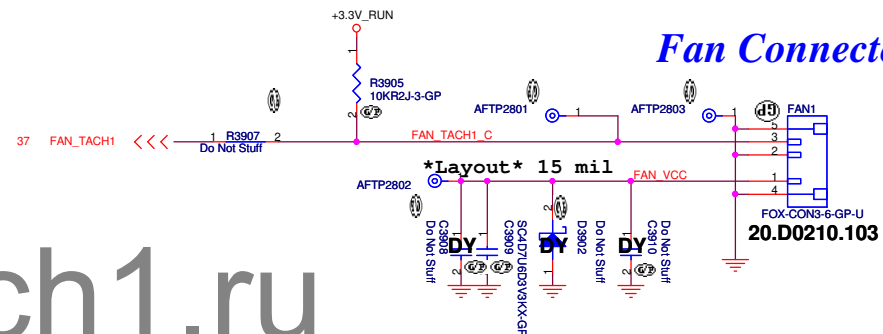
$$R(K\Omega) = 0.0012 * T^2 - 0.9308T + 96.147$$

## Fan controller

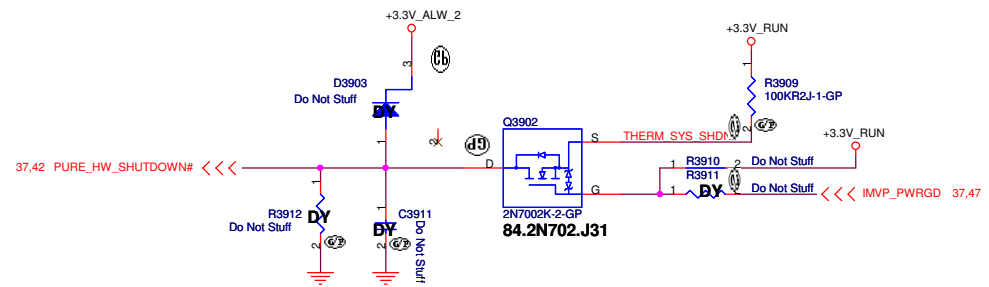


1st : 74.00991.031  
2nd : 74.02793.A31  
3rd : 74.05606.A71

## Fan Connector



20.D0210.103



DV15 CP UMA second

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Rev  
A00

Sheet 40 of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

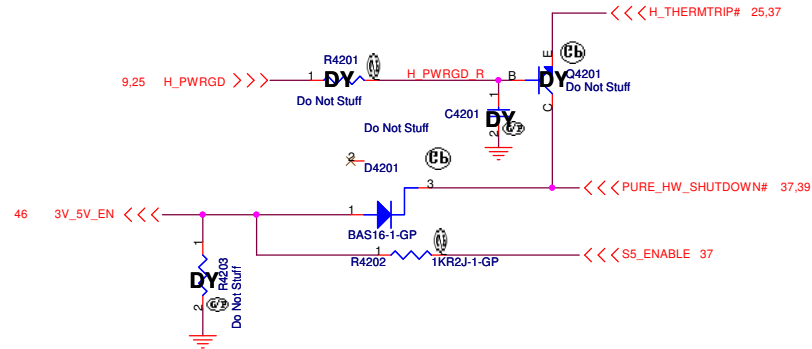
Size  
A3

Document Number  
Enrico/Caruso 15 CP

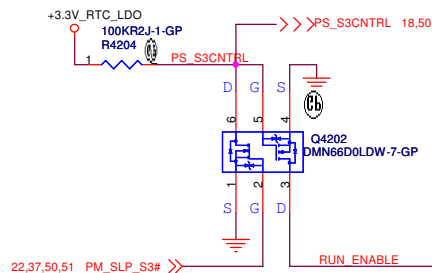
Rev  
A00

Date: Friday, April 08, 2011Sheet 41 of 99

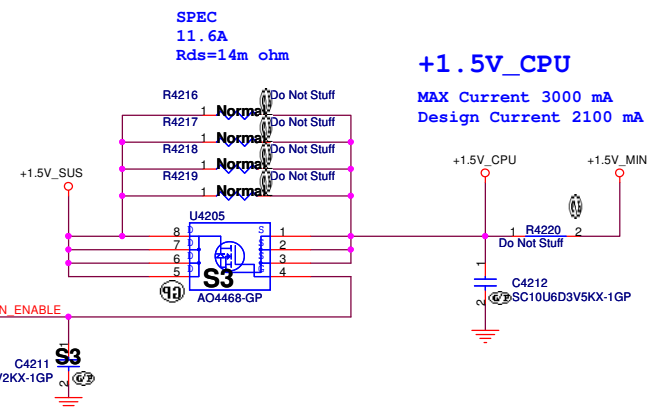
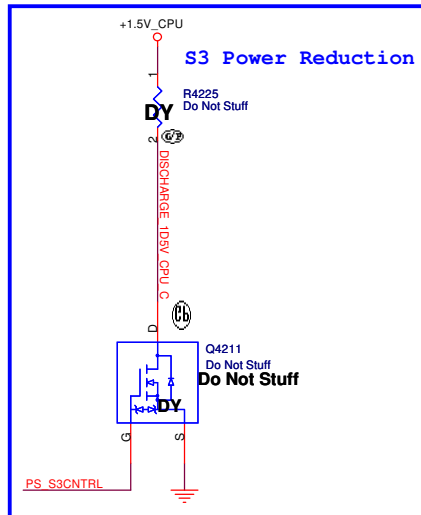
**SSID = Reset.Suspend**



## Run Power



www.aitech1.ru



**+1.5V\_CPU Consumption**  
MAX Current 3000 mA  
Design Current 2100 mA

**+1.5V\_MINI for Mini-Card Consumption**  
Peak current 1A

**Total= 4A**

DV15 CP UMA second

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

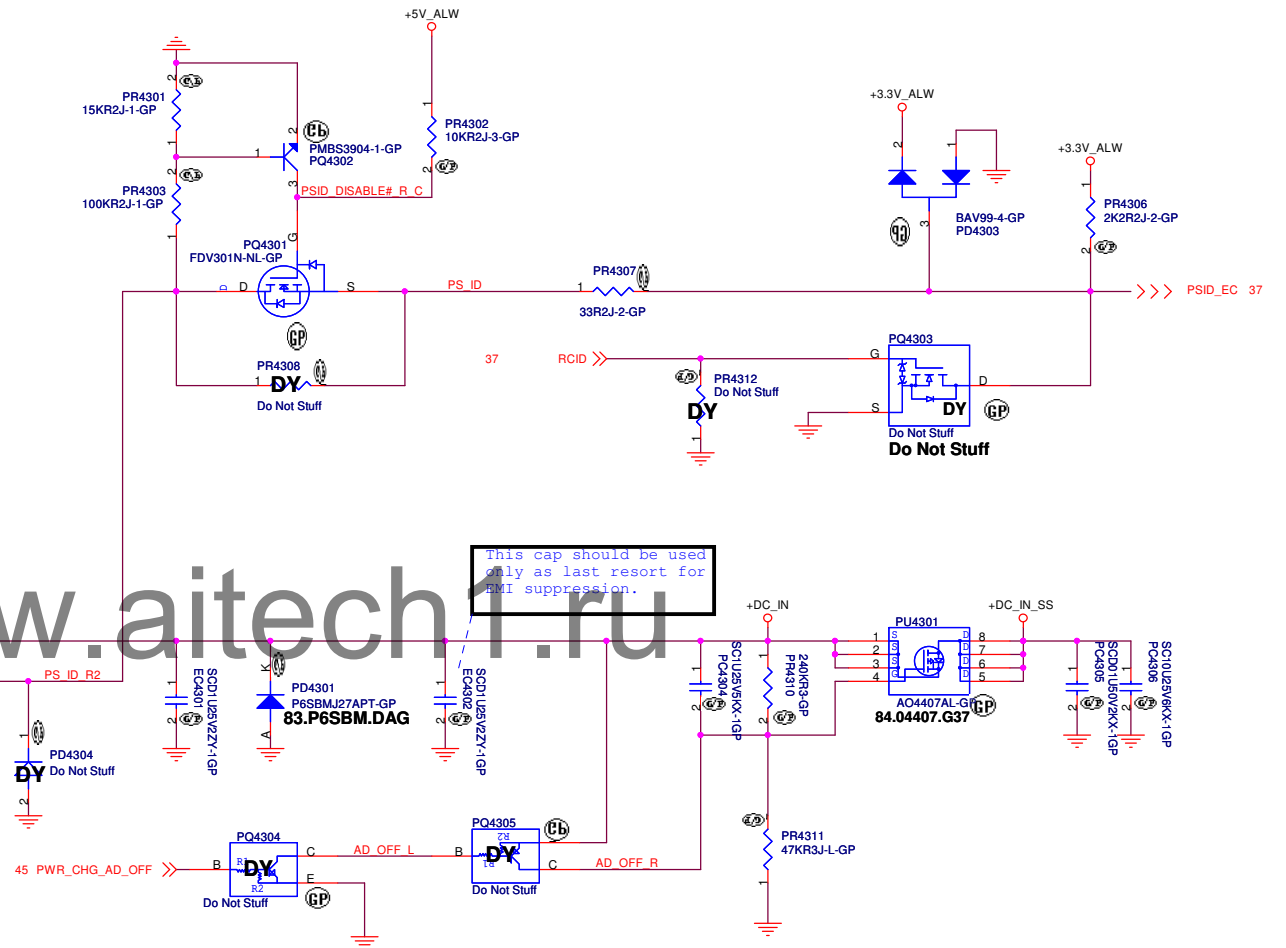
Title: **Power Plane Enable**  
Size: A3 Document Number: **Enrico/Caruso 15 CP** Rev: **A00**  
Date: Wednesday, April 13, 2011 Sheet: 42 of 99

SSID = PWR.Support

## DCin CONN

remove EL4301 for  
current rating

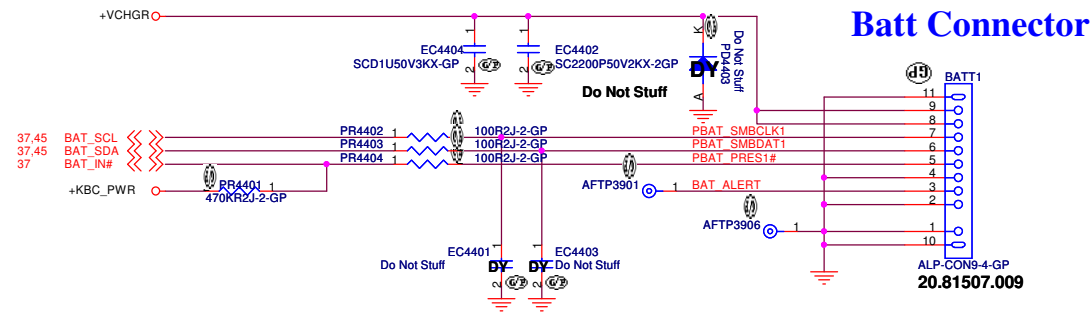
Follow DW50



This cap should be used  
only as last resort for  
EMI suppression.

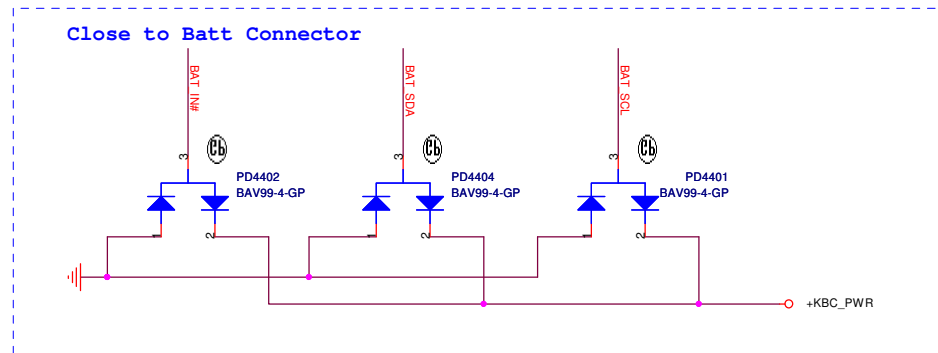
DV14 CP

SSID = BATT CONN



www.ditech1.ru

For actual location, need to be swap all pin

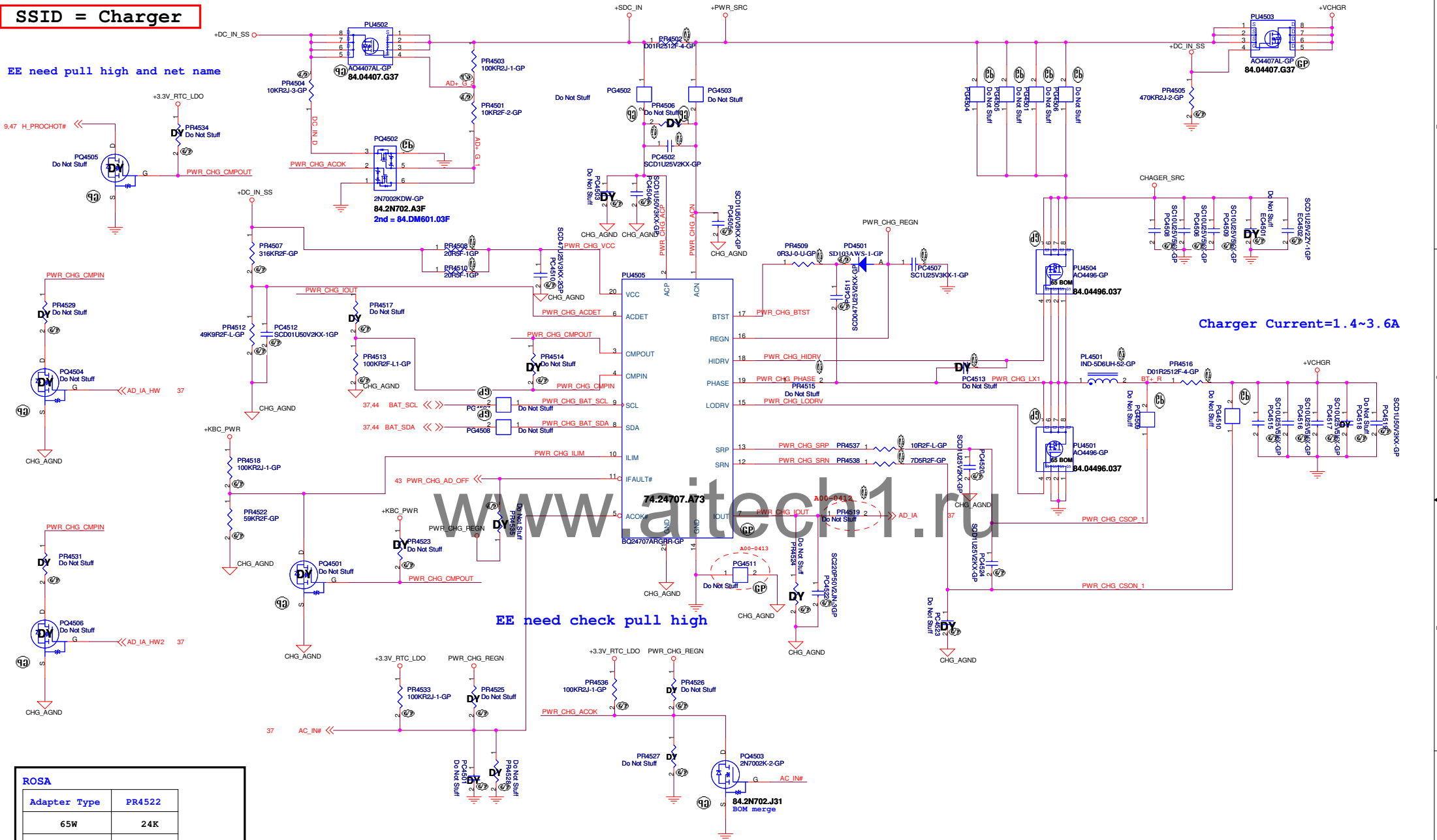


<Core Design>



SSID = Charger

EE need pull high and net name



EE need check pull high

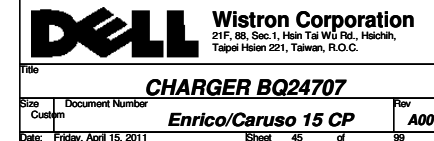
Charger Current=1.4~3.6A

Adapter Type	PR4522
65W	24K
90W	33.2K
130W	59K

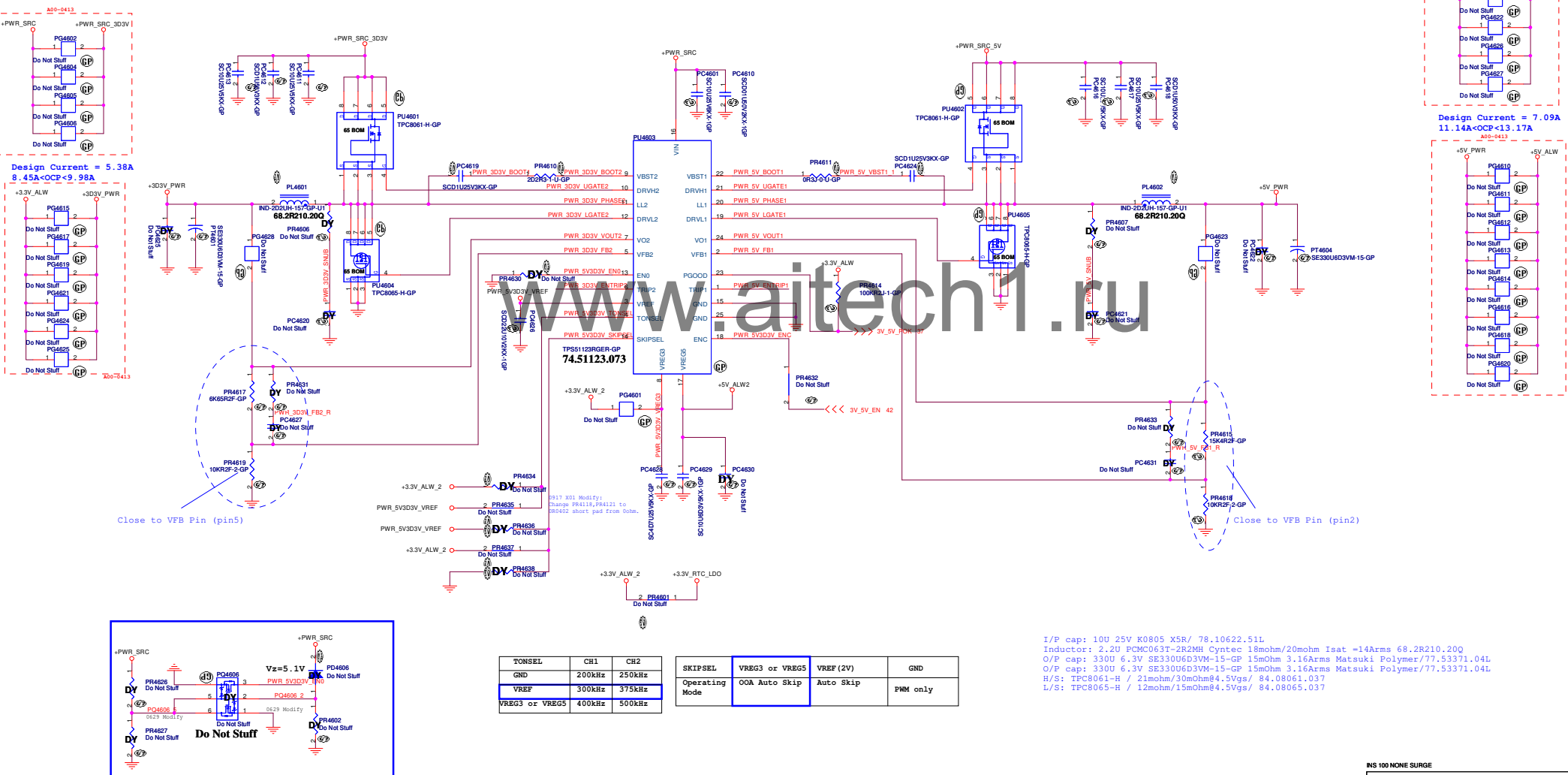
EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

**<Core Design>**



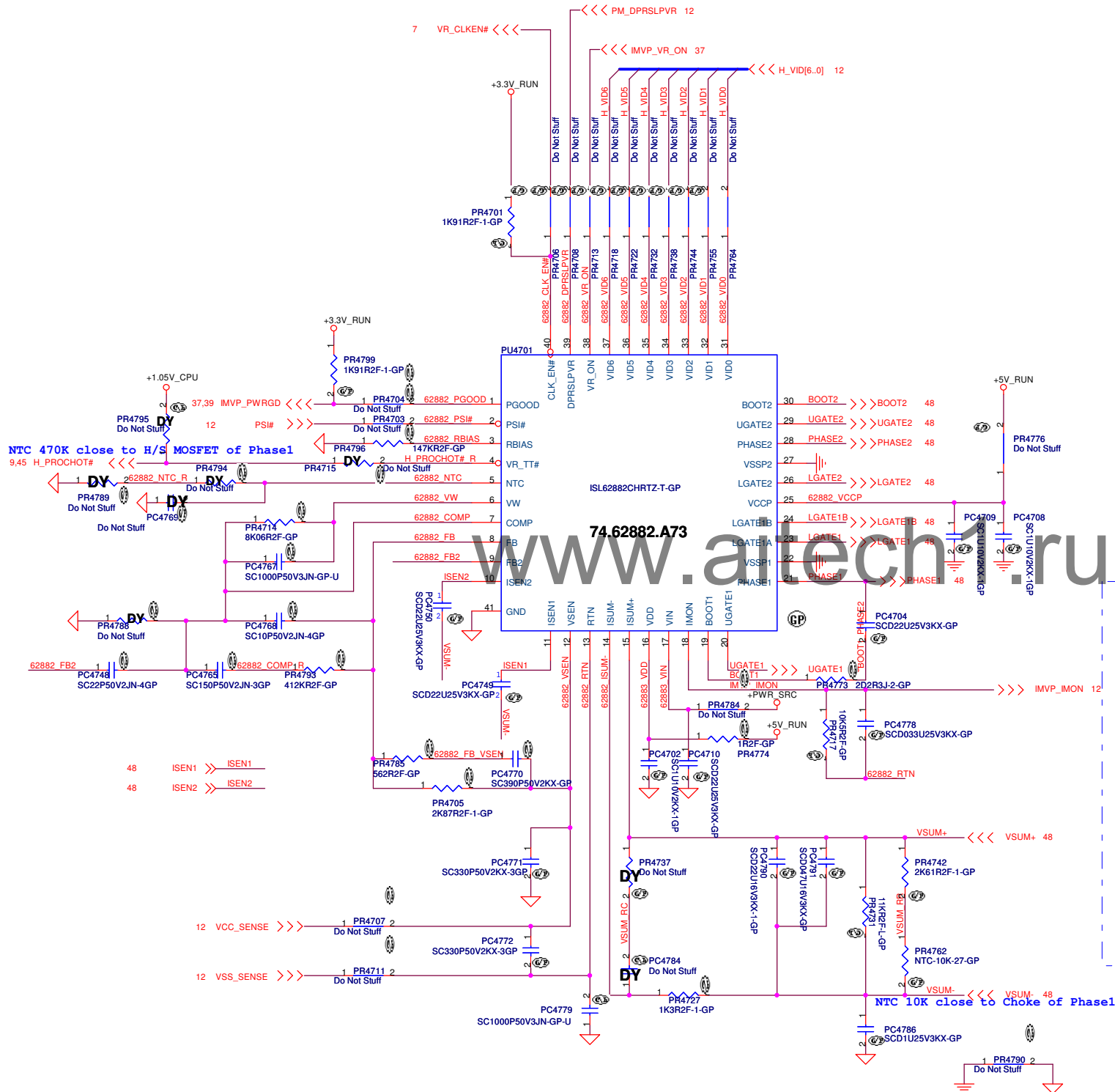
SSID = PWR.Plane.Regulator\_5v3p3v



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

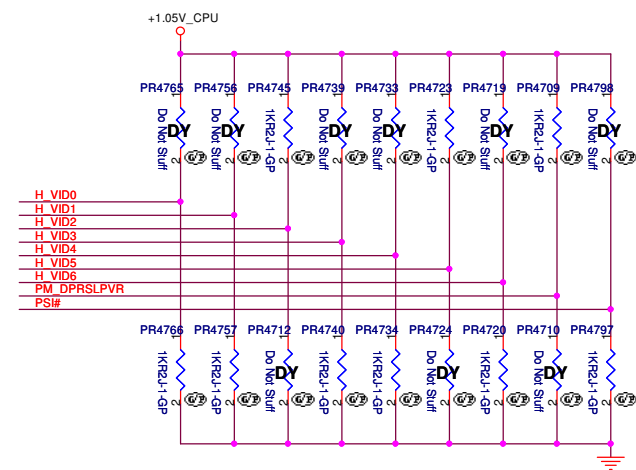
SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.200  
O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L  
O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L  
H/S: TPC8061-H / 21mohm/30mOhm4.5Vgs/ 84.08061.037  
L/S: TPC8065-H / 12mohm/15mOhm4.5Vgs/ 84.08065.037

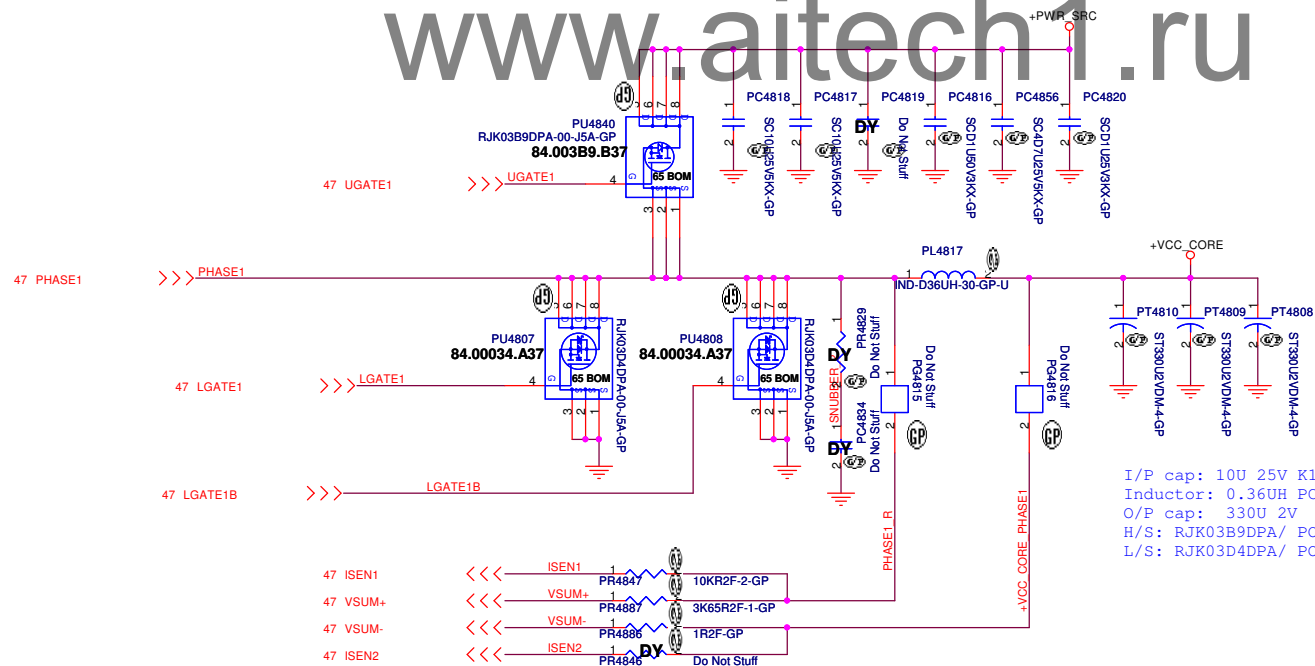
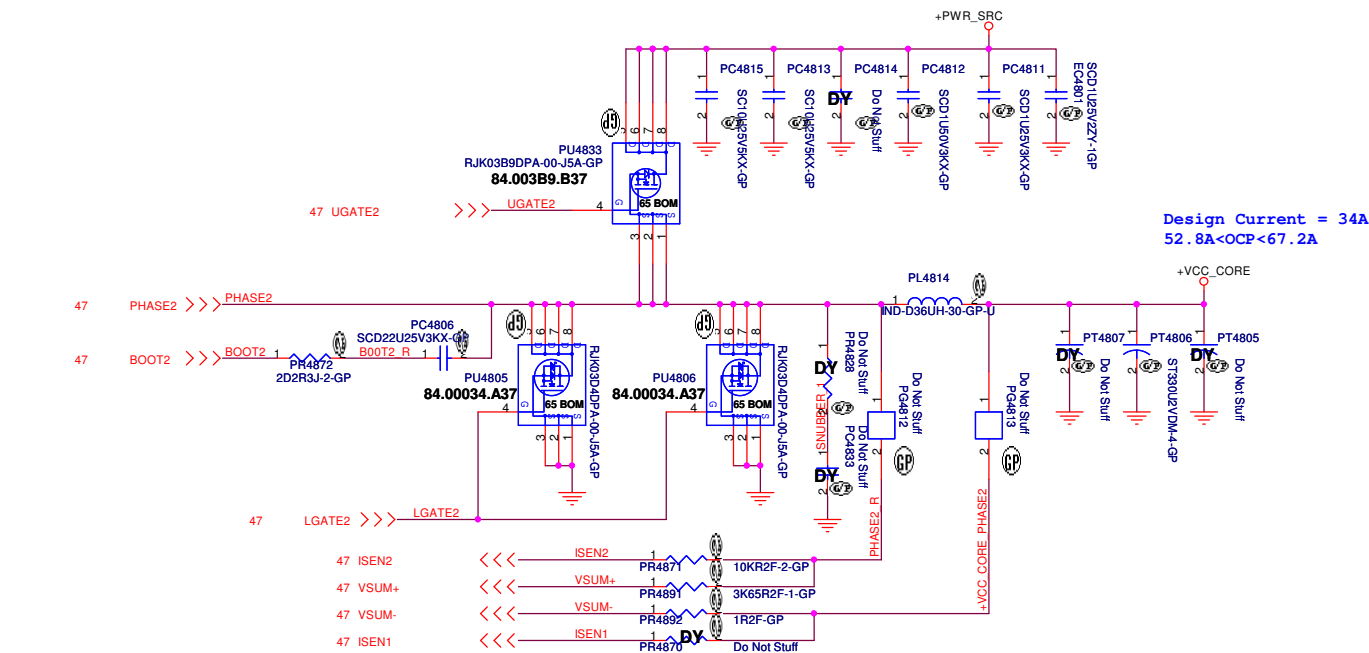


+PWR\_SRC  
TC4705  
Do Not Stuff  
remove TC4704 for layout

Intel support POC (power on current).



DV15 CP UMA second



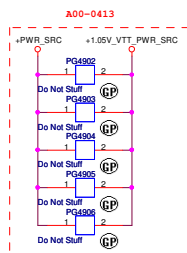
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.36UH PCMC104T-R36MN1R05J Cynotec 1.05mohm/ 68.R3610.20C  
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37  
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 CP UMA second

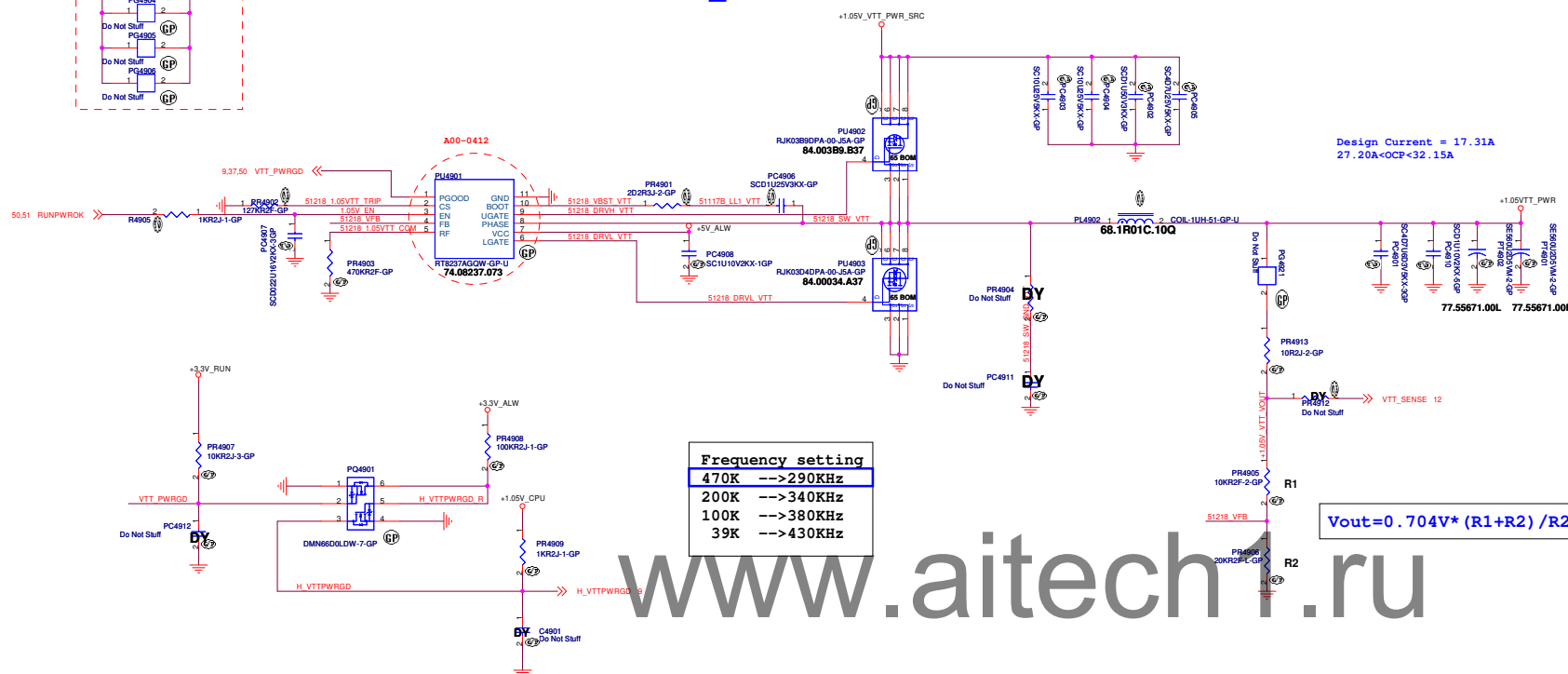


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>ISL62883 CPU CORE</b>		
Size	Document Number	Rev
A3	<b>Enrico/Caruso 15 CP</b>	<b>A00</b>
Date:	Wednesday, April 13, 2011	Sheet 48 of 99



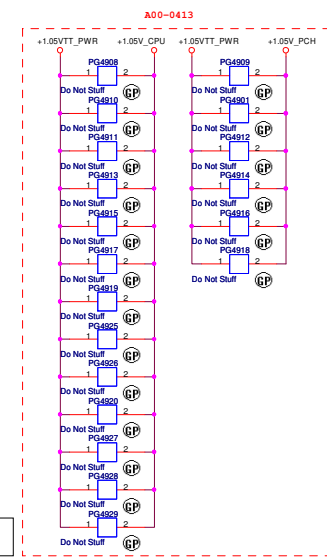
## RT8237A for +1.05V\_VTT



Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

Design Current = 17.31A  
27.20A<OCP<32.15A

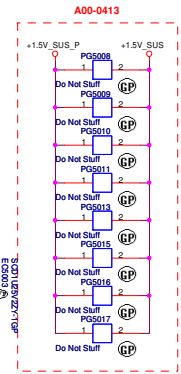
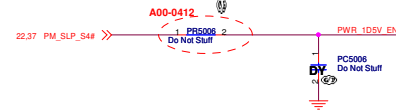
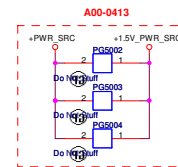
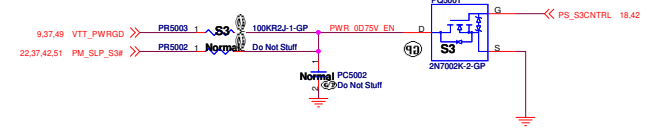
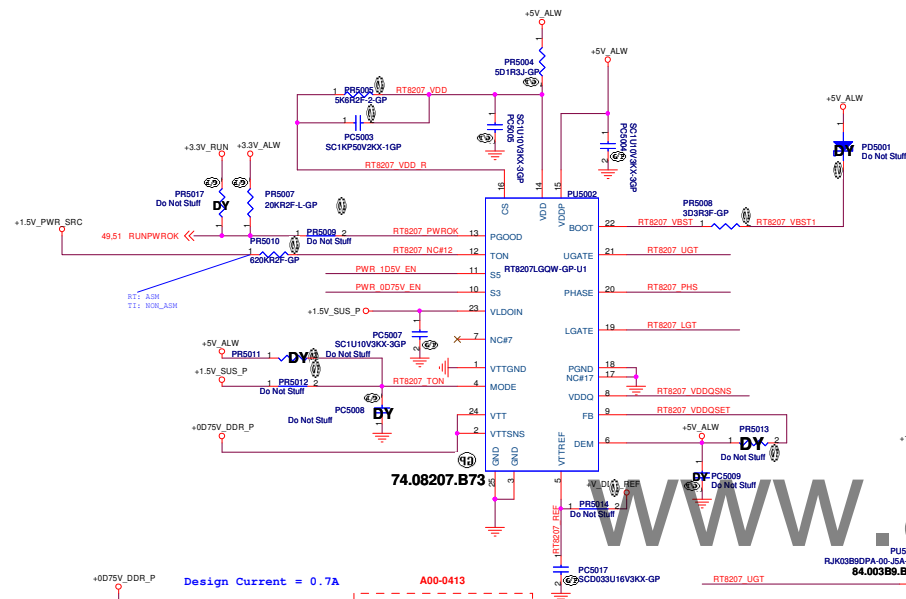
$$V_{out} = 0.704V * (R1 + R2) / R2$$



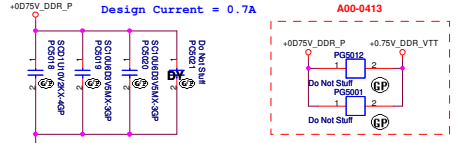
www.aitech1.ru

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 10H PCMC104T-1R0MH Cyntec 3mohm/3.3mohm Isat +28Arms 68.1R01C.100  
O/P cap: CHIP CAP POL 560U 2.5V 6.3\*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L  
O/P cap: CHIP CAP POL 560U 2.5V 6.3\*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37  
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mOhm@4.5Vgs/ 84.00034.A37

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



Design Current = 7.35A  
11.55A<OCP<13.65A

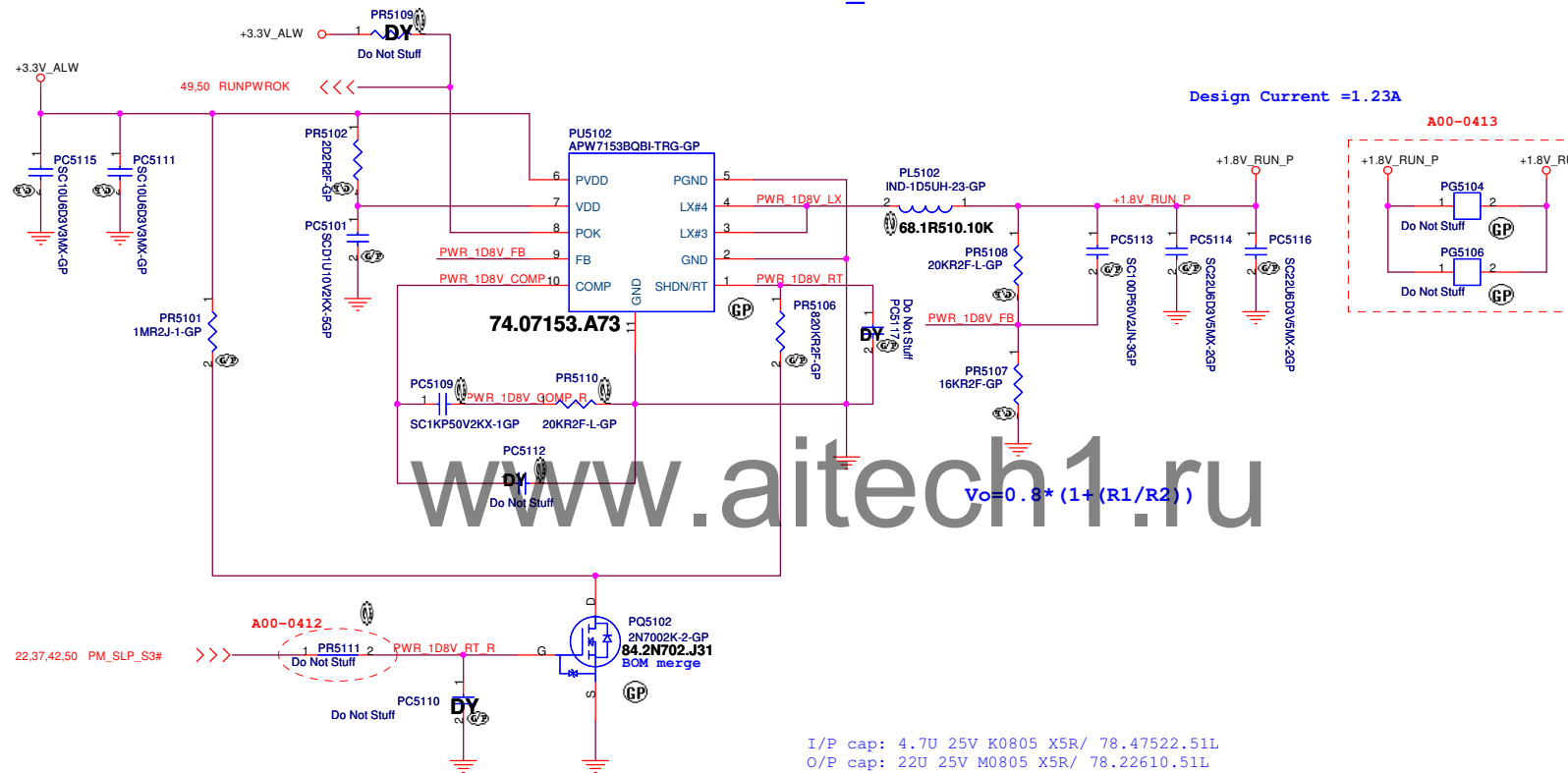


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 1.5U PFCM140T-1R5MH Cyntec 3.8mohm/4.2mohm Isat ~33Arms 68.1R510.10J  
O/P cap: C1P1 C1P1 POL 2.5V 6.3V 7 15mOhm 3.5Arms Matsuk/77.55671.00L  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/1.51mOhm8.4Vgvs/ 84.003B9.337  
L/S: RJK034DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm8.4Vgvs/ 84.00034.A37

# APW7153B for 1D8V\_RUN



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L  
 O/P cap: 22U 25V M0805 X5R/ 78.22610.51L  
 Inductor: CHIP CHOKE 1.5U PCMC063T-1R5MN Cynotec 14mohm/15mohm Isat =18Arms 68.1R510.10K

INS 100 NONE SURGE

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>APW7153B for 1D8V RUN</b>			
Size A3	Document Number	Rev	
<b>Enrico/Caruso 15 CP</b>		<b>A00</b>	
Date: Friday, April 15, 2011		Sheet 51 of 99	

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

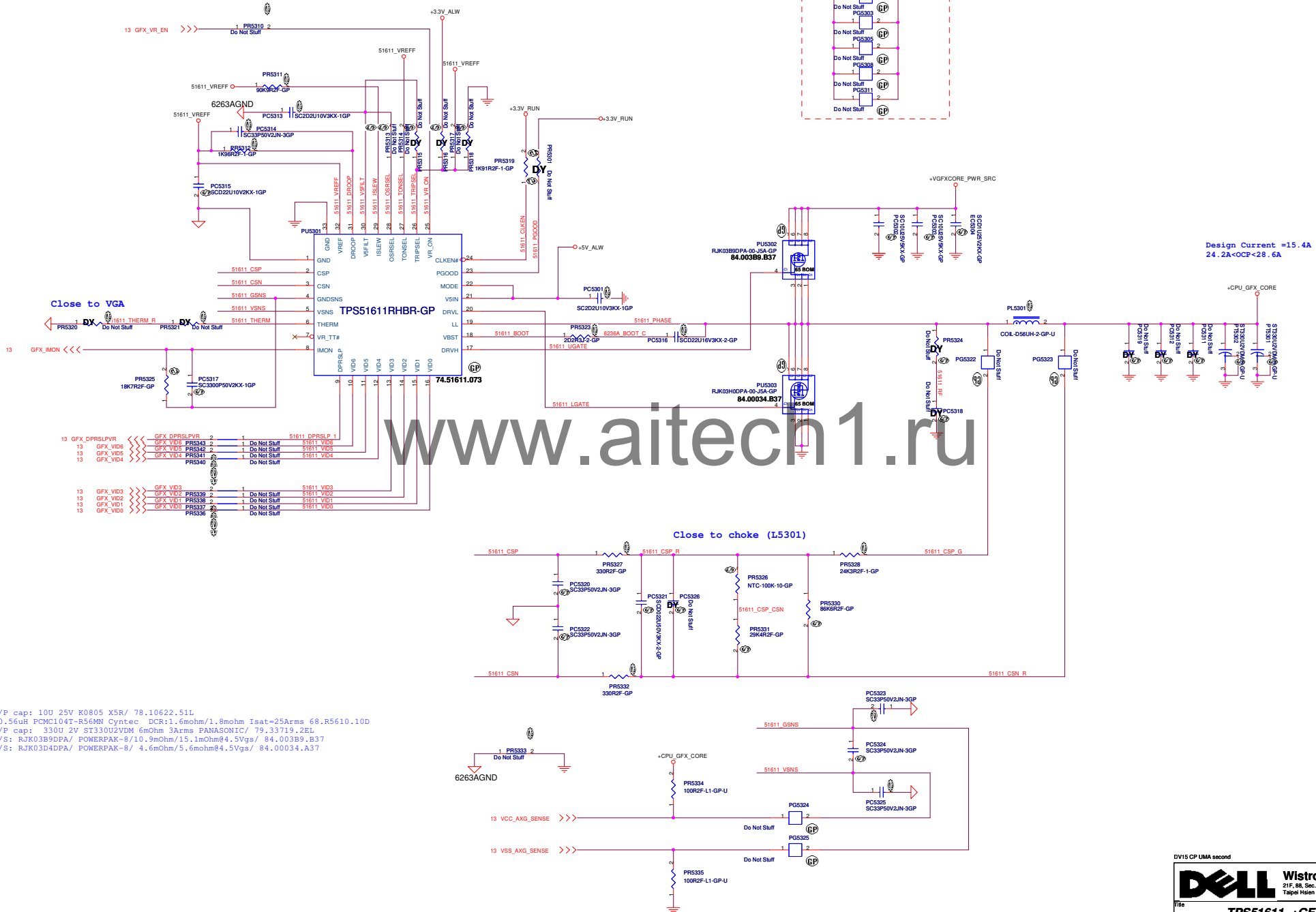
Document Number  
Enrico/Caruso 15 CP

Rev  
A00

Date: Friday, April 08, 2011Sheet 52 of 99



SSID = CPU.GFX.Regulator



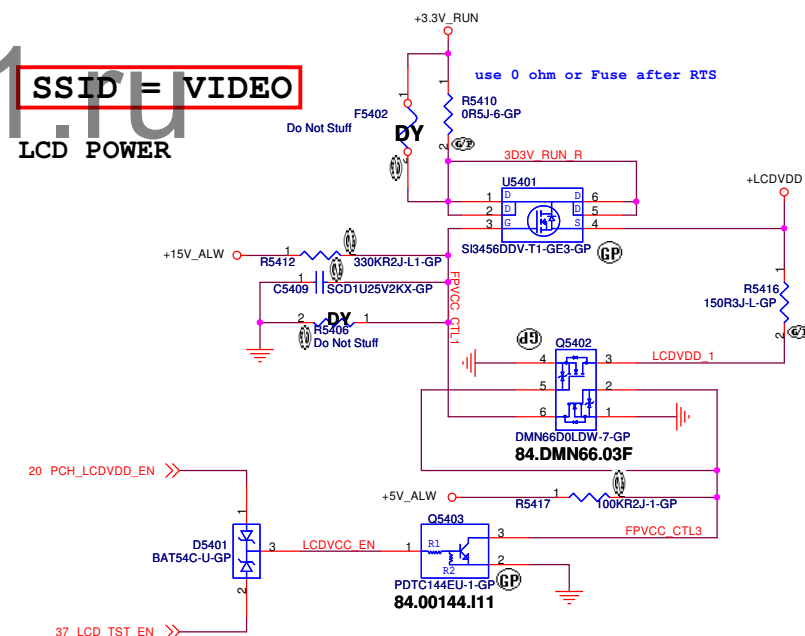
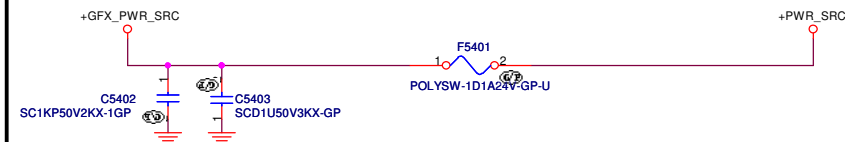
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
I/O.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 330U 2V TI330U2VDM 6mOhm 3Arms PANASONIC/ 79.33719.2EL  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm/4.5Vgs/ 84.003B9.B37  
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm/4.5Vgs/ 84.00034.A37

DV16 CP UMA second

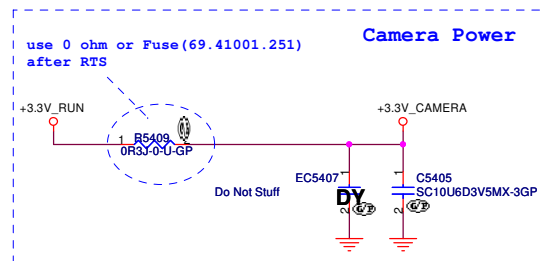
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>TPS51611_+GFX_CORE</b>			
Size A2	Document Number	Rev	
<b>Enrico/Caruso 15 CP</b>		<b>A00</b>	
Date:	Wednesday, April 13, 2011	Sheet	53 of 99

**SSID = Inverter**

## INVERTER POWER



## Camera Power



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

### LCD/Inverter Connector

Size  
A3

Document Number

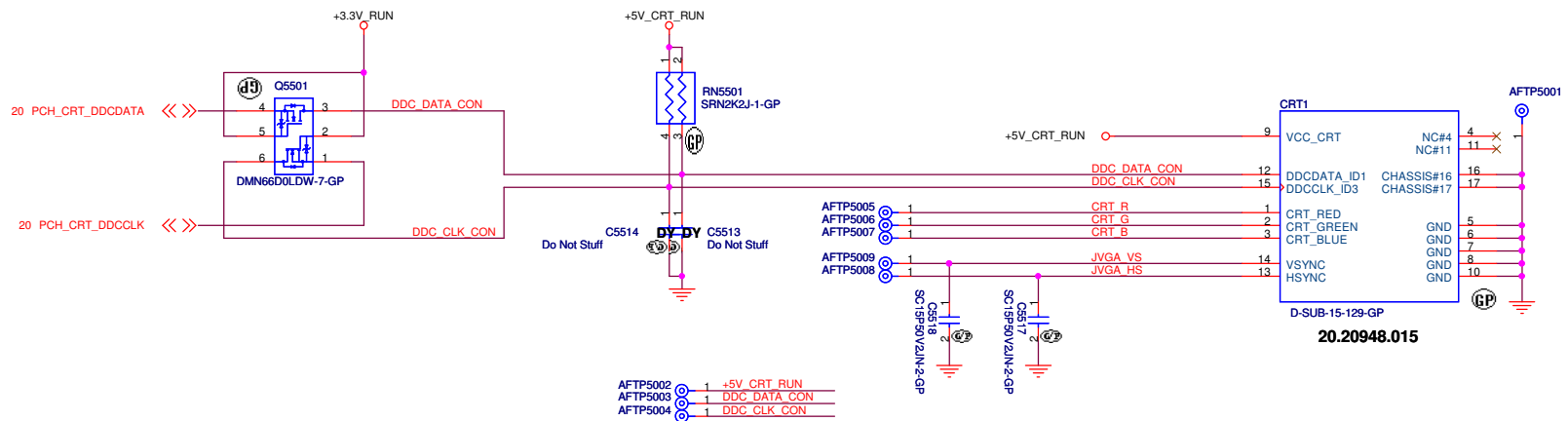
**Enrico/Caruso 15 CP**

Rev	400
-----	-----

Date: Wednesday, April 13, 2011

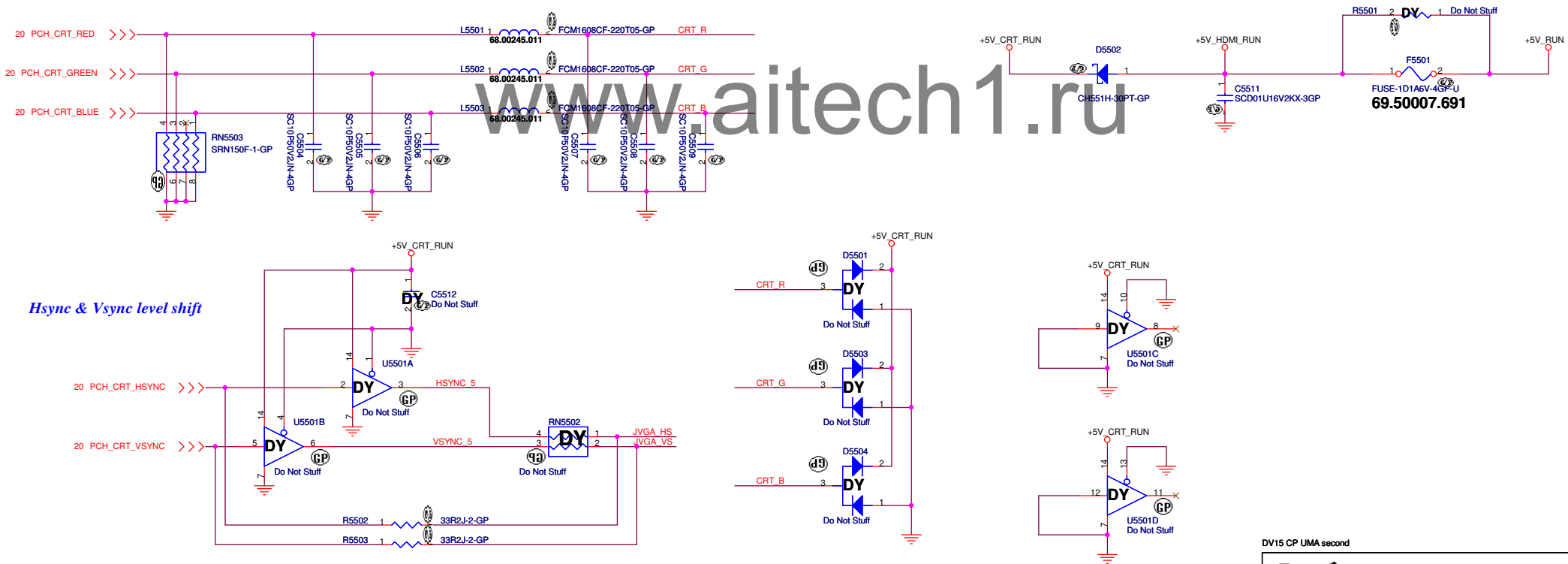
Sheet 54 of 9

**SSID = VIDEO**



**Layout Note:**

- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.




DV15 CP UMA second

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>CRT Connector</b>		
Size	Document Number	Rev
	<b>Enrico/Caruso 15 CP</b>	<b>A00</b>
Date:	Wednesday, April 13, 2011	Sheet 55 of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second

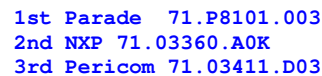
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A3	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011	Sheet	56	of 99

## *HDMI Level Shifter & CONNECTOR*

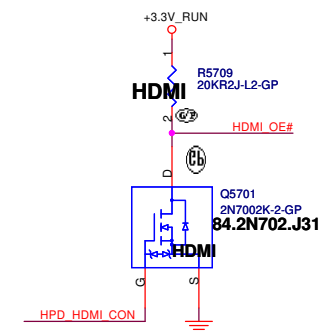


		PS8101	PTN3360B	PI3VDP411LS
PIN3	R5703	Stuff 4.7K_5%	DY	DY
PIN4	R5704	DY	DY	DY
	R5706	DY	DY	Stuff 200K_5%
PIN6	R5705	Stuff 499_1%	Stuff 10K_1%	DY
PIN10		NC	NC	NC

## HDMI CONN



**A00-0412**



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

## HDMI Level Shift/ Connector

Size

Document Number

**Enrico/Caruso 15 CP**

Date: Wednesday, April 13, 2011

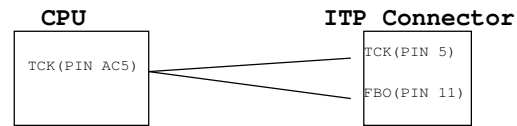
Sheet 57 of 99

Rev  
A00

```
SSID = User.Interface
```

## ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



www.aitech1.ru

## REMOVE FAN CONNECTOR FOR HR THERMAL SOLUTION 7/12

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

### ITP Connector

Size  
A3

Document Number
-----------------

**Enrico/Caruso 15 CP**

Rev

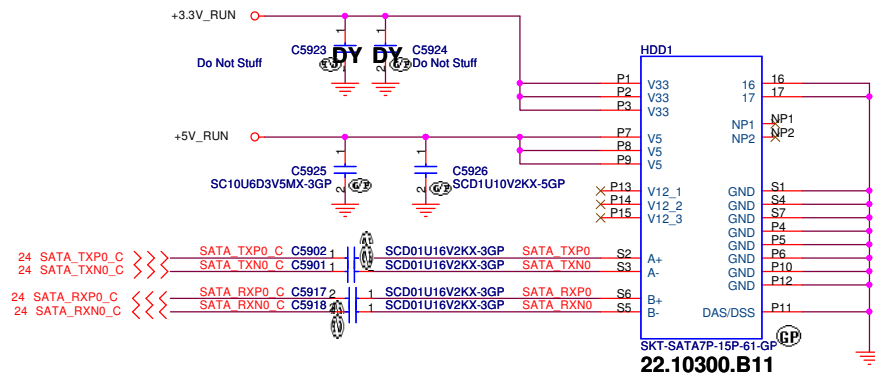
**A00**

Date: Friday, April 08, 2011

Sheet 58 of 99

SSID = SATA

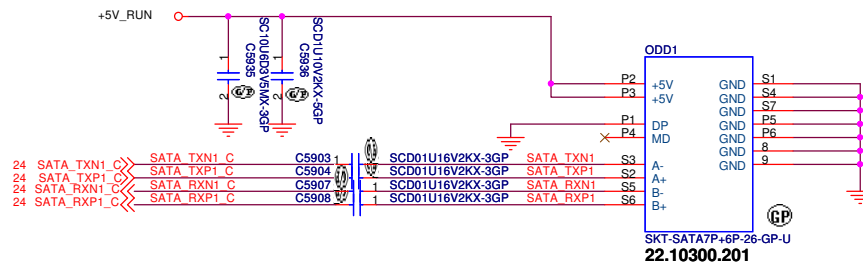
# SATA HDD Connector



www.aitech1.ru

# SATA ODD Connector

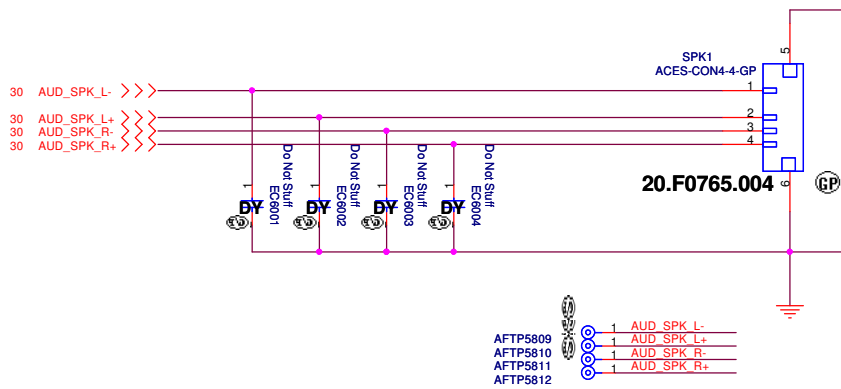
SATA\_RX- and SATA\_RX+ Trace  
Length match within 20 mil



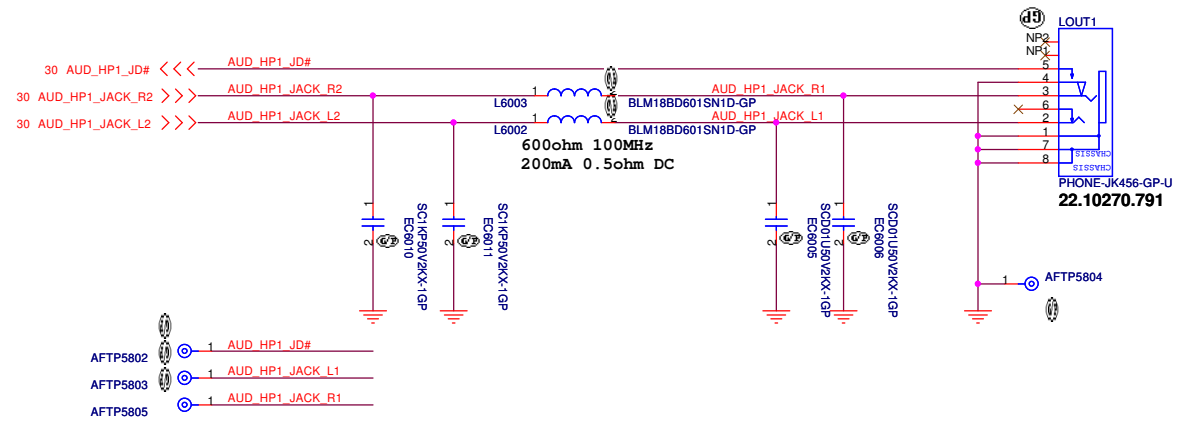
DV15 CP UMA second

SSID = AUDIO

## Speaker Connector

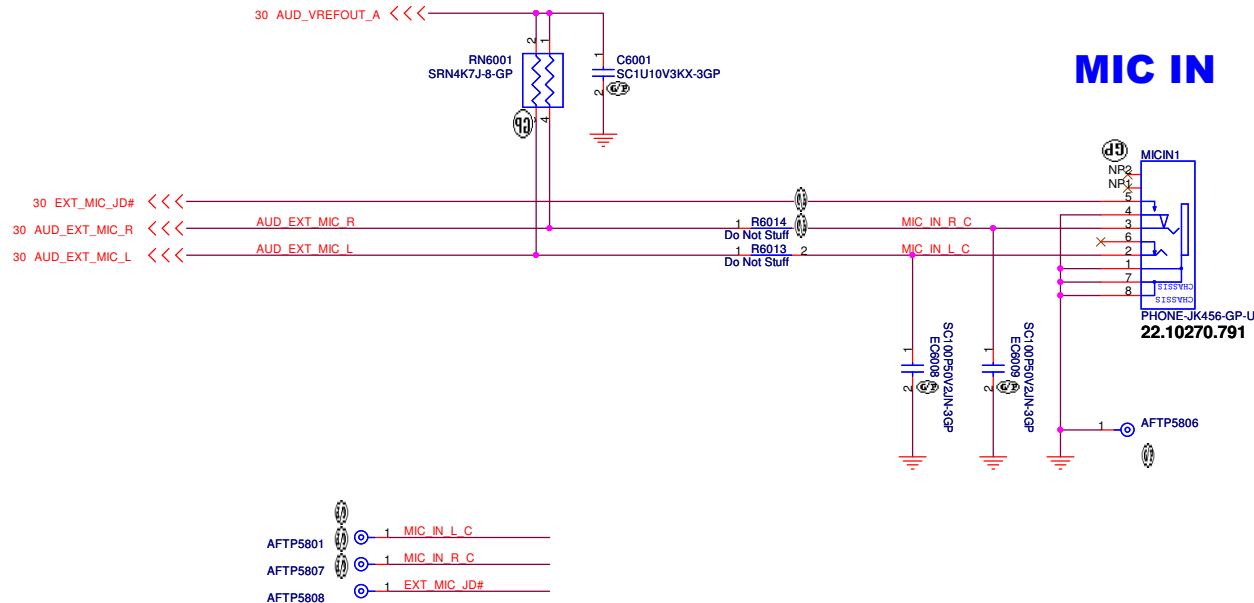


## LINE1 OUT

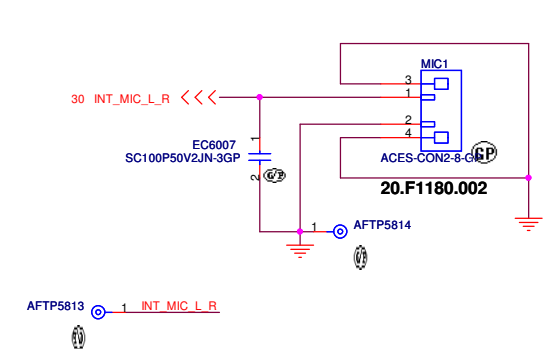


www.aitech1.ru

## MIC IN



## Internal Microphone



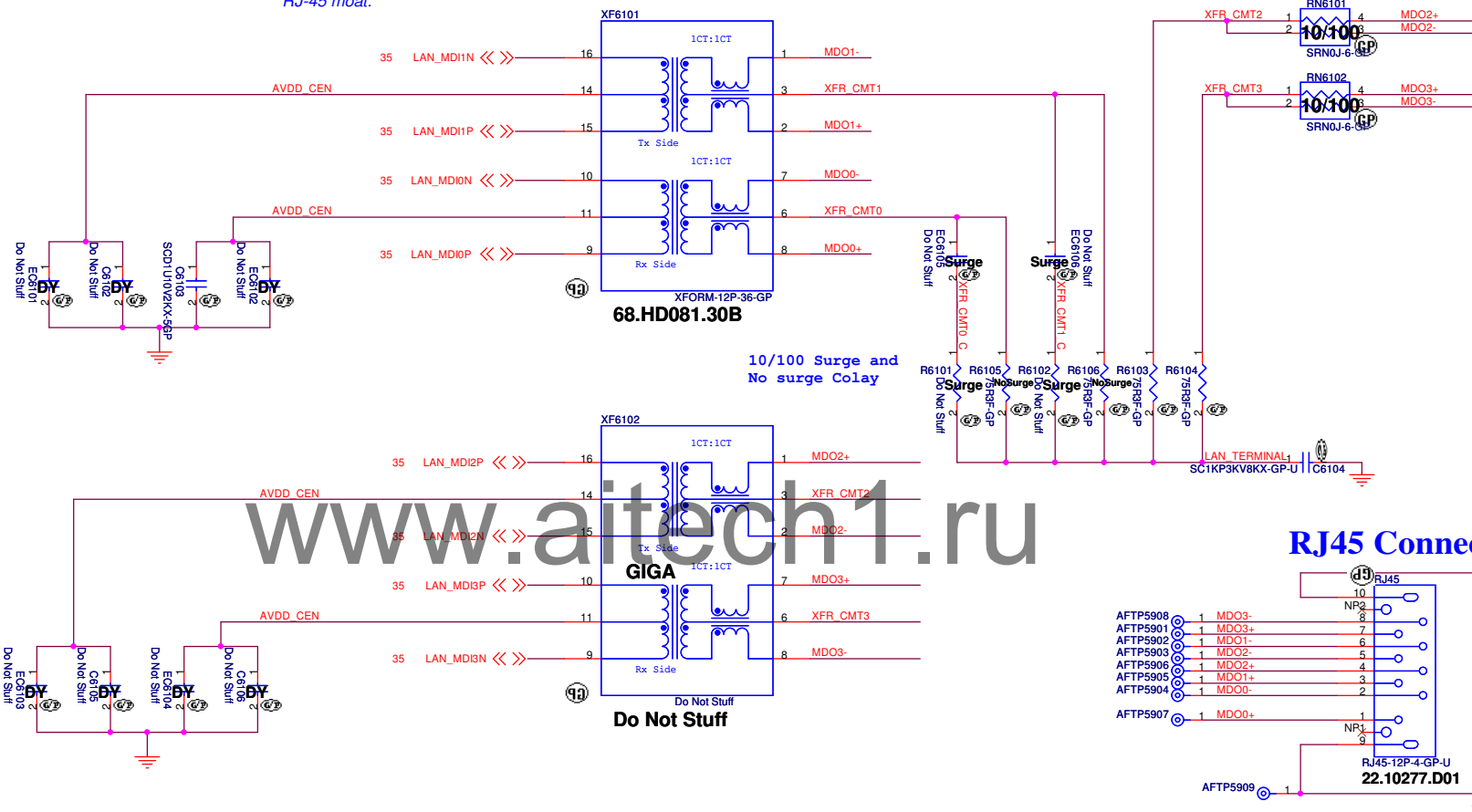
DV15 CP UMA second



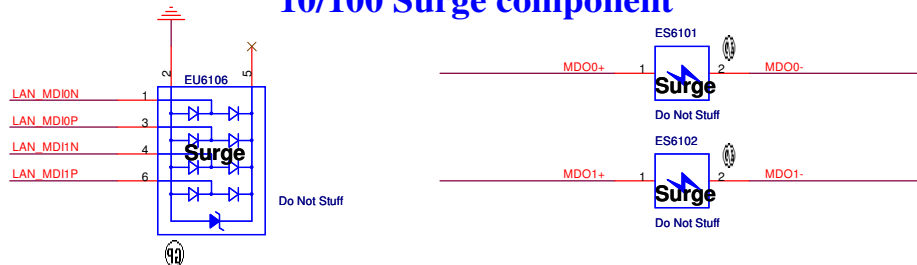
2009-10-1 Change MDI1+ (XF601.16) to MDI1+ (XF601.15)  
 Change MDI1- (XF601.15) to MDI1- (XF601.16)  
 Change MDI0+ (XF601.10) to MDI0+ (XF601.9)  
 Change MDI0- (XF601.9) to MDI0- (XF601.10)  
 Change RJ45-3 (XF601.1) to RJ45-3 (XF601.2)  
 Change RJ45-6 (XF601.2) to RJ45-6 (XF601.1)  
 Change RJ45-1 (XF601.7) to RJ45-1 (XF601.8)  
 Change RJ45-2 (XF601.8) to RJ45-2 (XF601.7)

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

## 10/100M Lan Transformer



## 10/100 Surge component



<Core Design>

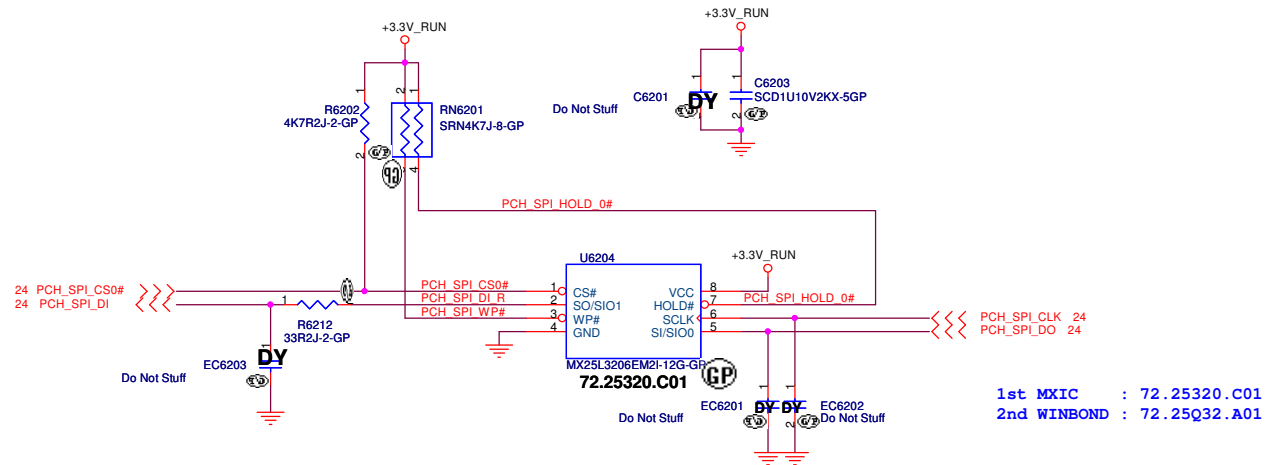


**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

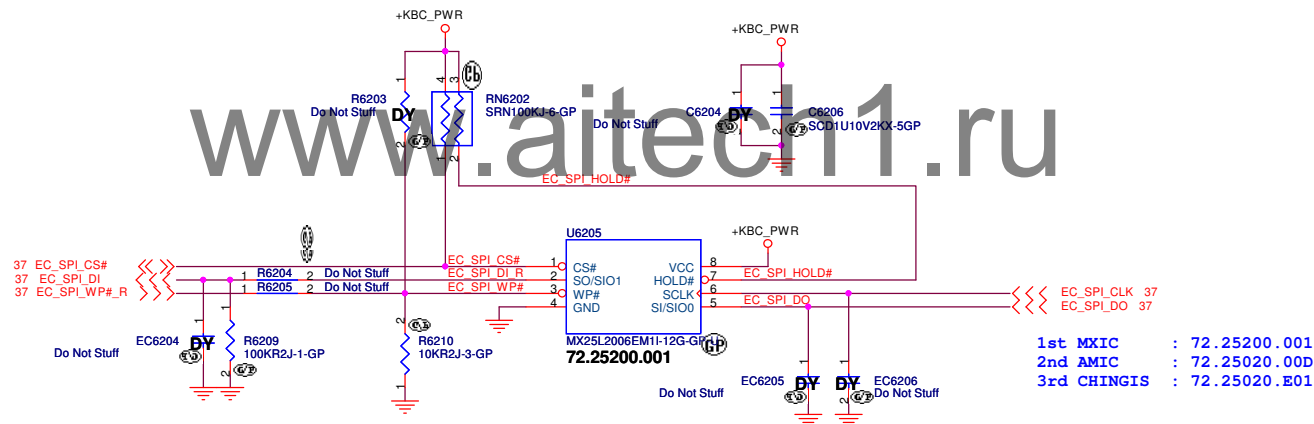
LAN Conn			
Size A3	Document Number	Enrico/Caruso 15 CP	
Date: Wednesday, April 13, 2011	Sheet 61	of 99	Rev A00

**SSID = Flash.ROM**

**SPI FLASH ROM (32M bits) for PCH**

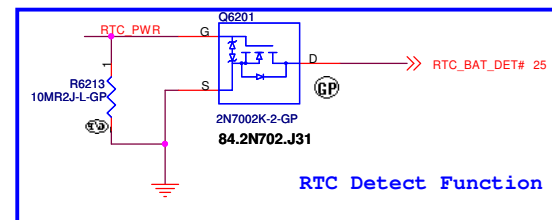
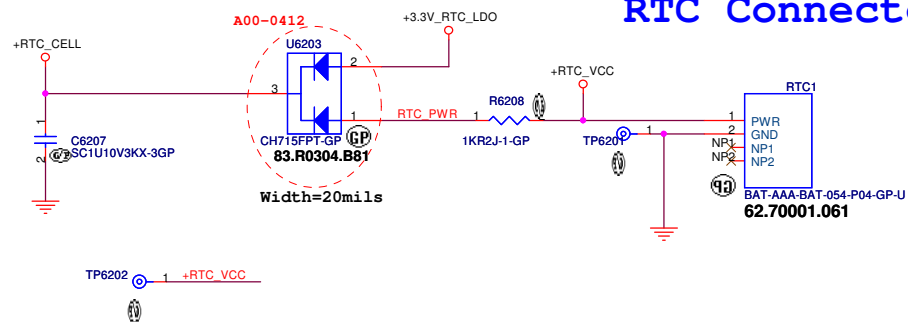


## SPI FLASH ROM (2M bits) for KBC



**SSID = RBATT**

## RTC Connector



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

### ***Flash/RTC***

Size  
A3

Document Number
-----------------

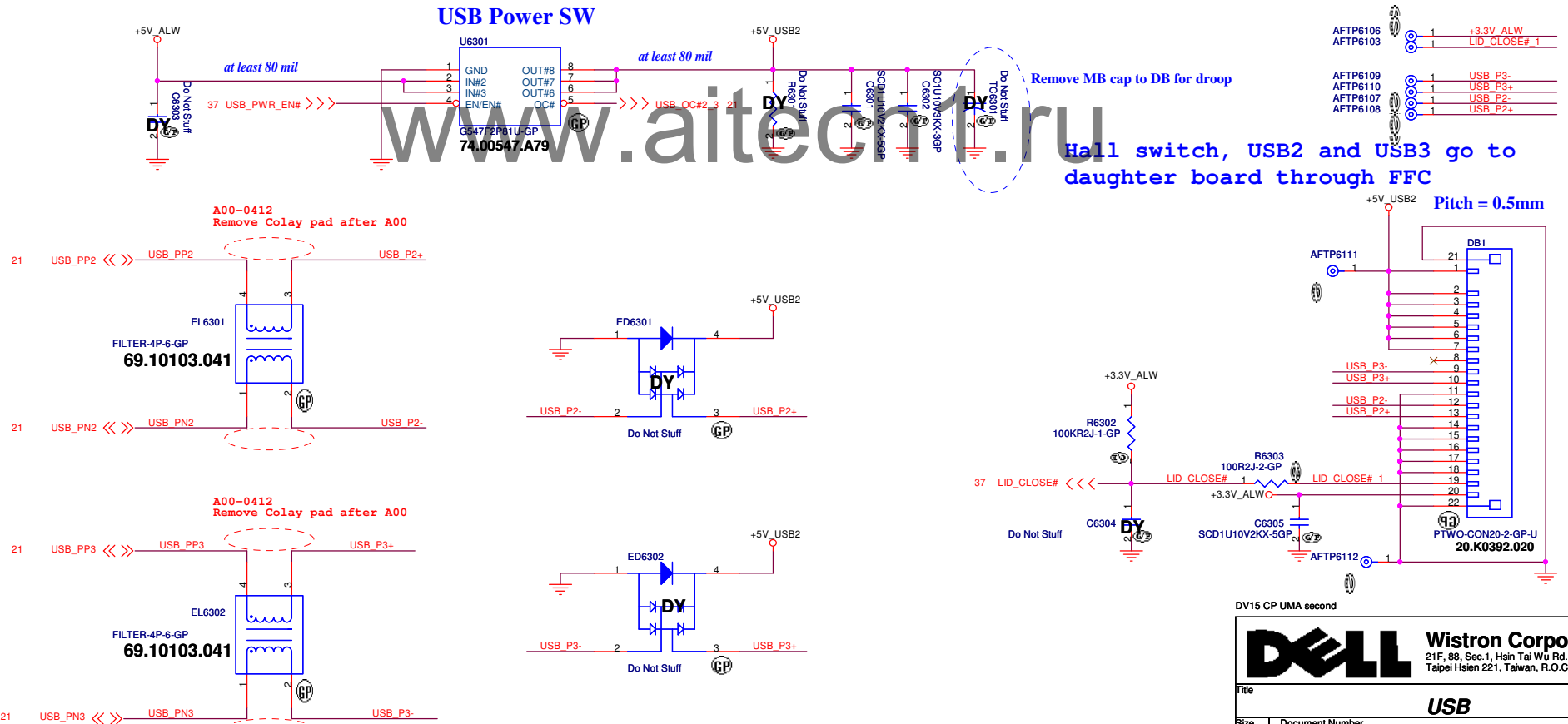
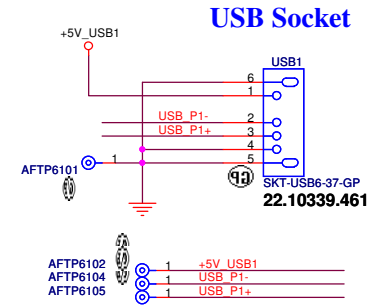
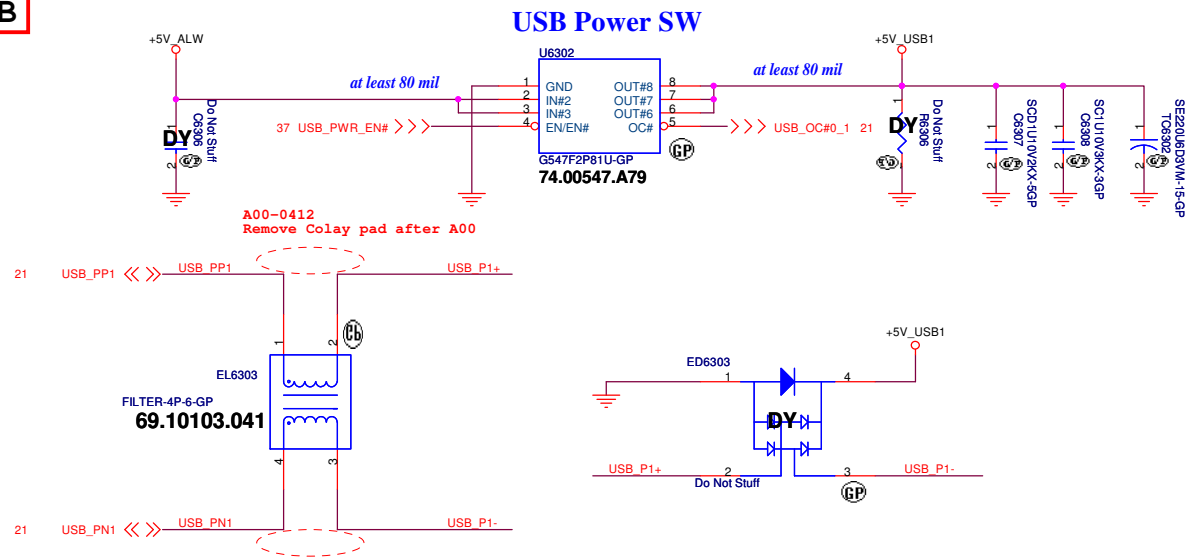
**Enrico/Caruso 15 CP**

Rev  
**A00**

Date: Wednesday, April 13, 2011

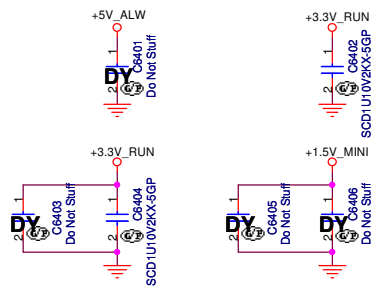
Sheet 62 of 99

SSID = USB



DV15 CP UMA second


### *Mini Card Connector(802.11a/b/g)*



(Blanking)

www.aitech1.ru

DV15 CP UMA second



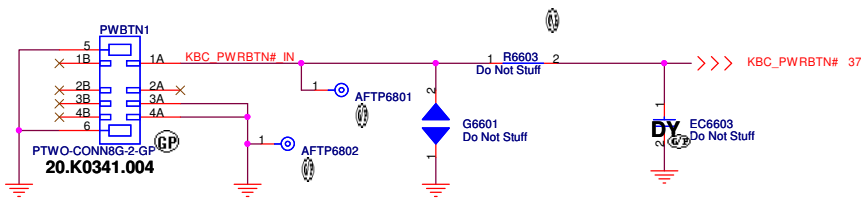
Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

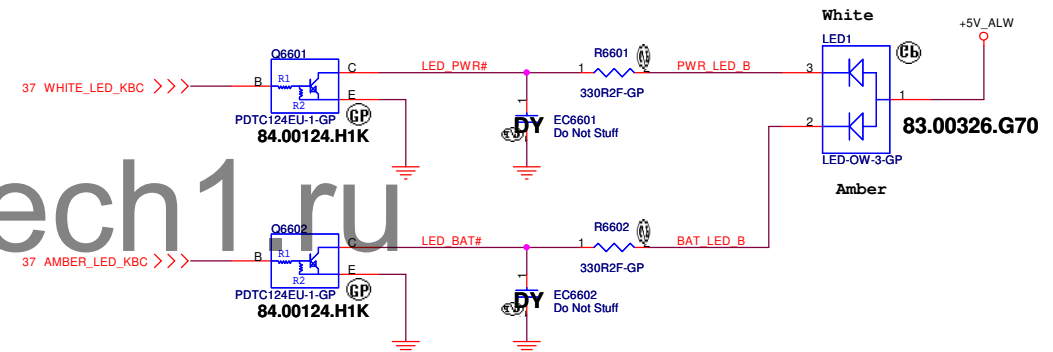
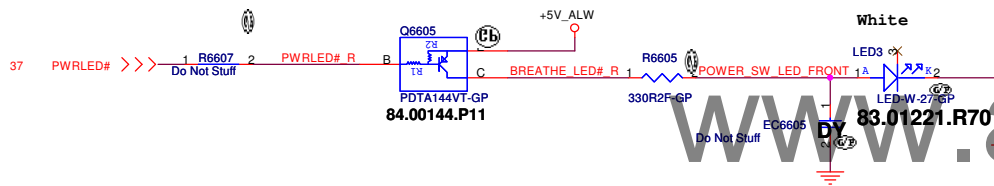
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011		Sheet 65 of 99

## Power BTN Connector

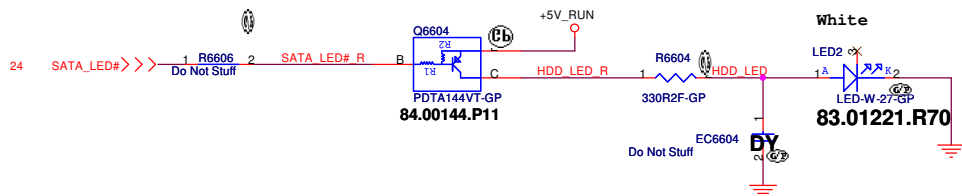


LED3      LED2      LED1      LED4  
 PWR      HDD      Battery      WLAN

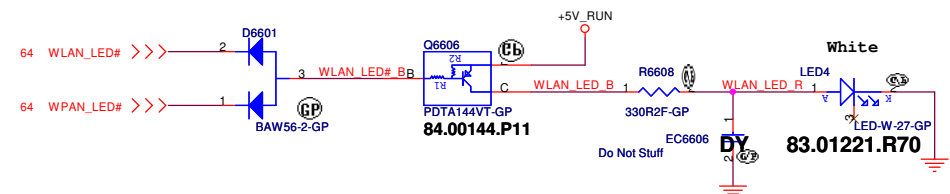
## Battery LED



## HDD LED



## WLAN LED



DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**LED**

Size  
A3

Document Number
-----------------

**Enrico/Caruso 15 CP**

Rev  
**A00**


Date: Wednesday, April 13, 2011

Sheet	66	of	99
-------	----	----	----

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
Enrico/Caruso 15 CP

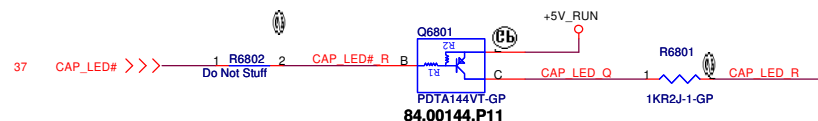
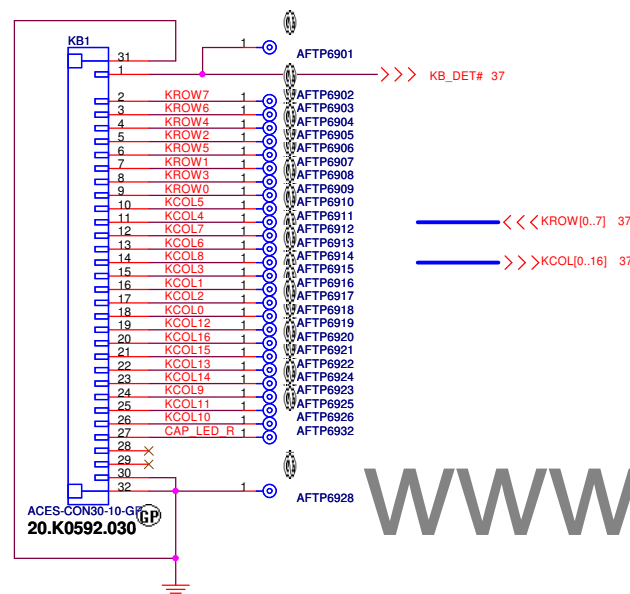
Date: Friday, April 08, 2011

Rev  
A00

Sheet 67 of 99

SSID = KBC

## Internal Keyboard Connector





www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

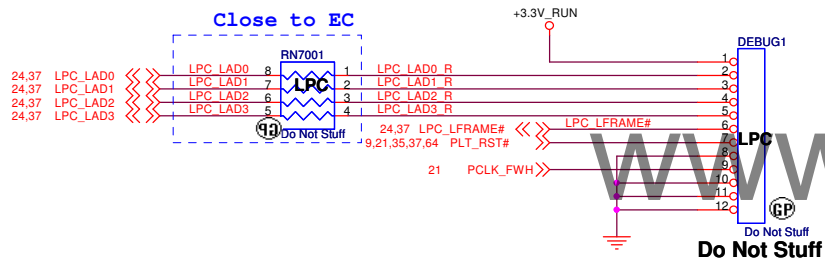
Size  
A3

Document Number  
Enrico/Caruso 15 CP

Rev  
A00

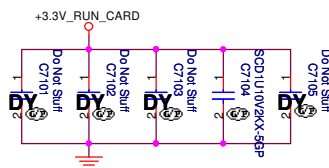
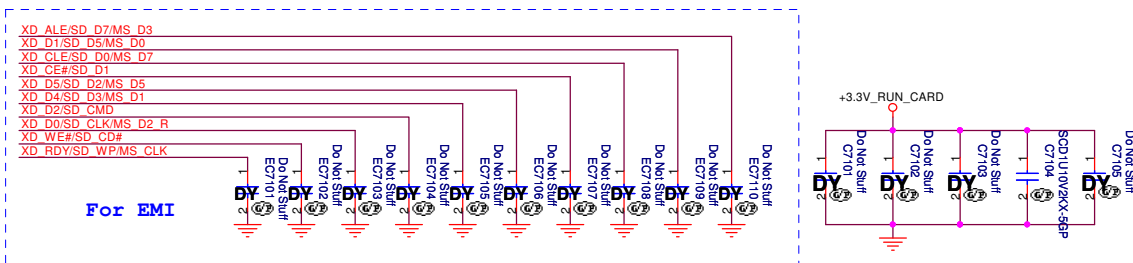
Date: Friday, April 08, 2011

Sheet 69 of 99



DV15 CP UMA second

## *SD/XD/MS Card Reader*



 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b><i>CDR Reader Connector</i></b>	
Size A3	Document Number <b><i>Enrico/Caruso 15 CP</i></b>
Date: Wednesday, April 13, 2011	Sheet 71 of 99 <b><i>A00</i></b>

(Blanking)  
www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

Rev  
**A00**

**RESERVED**

Sheet 72 of 99

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Reserved**  
**Enrico/Caruso 15 CP**


Rev  
**A00**

Date: Friday, April 08, 2011Sheet 73 of 99

(Blanking)

www.aitech1.ru


DV15 CP UMA second

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A3	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011	Sheet	74	of 99

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
Enrico/Caruso 15 CP

Rev  
A00

Date: Friday, April 08, 2011Sheet 75 of 99

www.aitech1.ru

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

Rev  
**A00**


**Reserved**

Sheet 76 of 99



(Blanking)  
www.aitech1.ru

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size A3	Document Number <b>Enrico/Caruso 15 CP</b>	Rev <b>A00</b>
------------	---	-------------------

Date: Friday, April 08, 2011	Sheet 77 of 99
------------------------------	----------------

(Blanking)

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

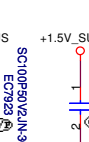
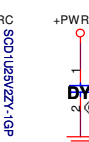
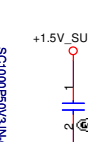
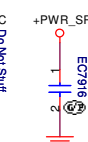
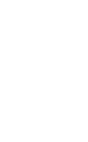
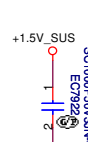
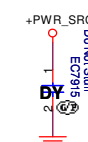
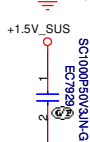
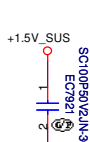
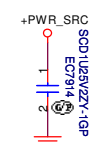
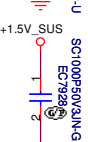
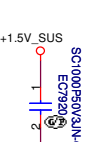
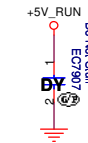
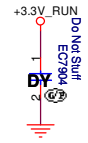
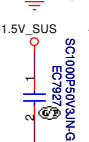
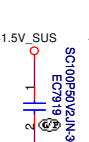
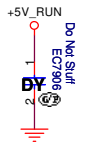
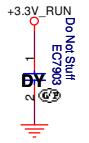
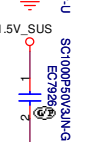
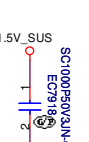
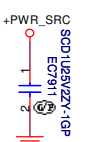
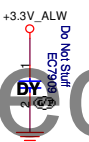
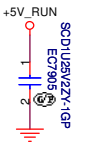
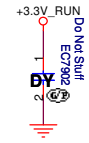
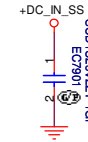
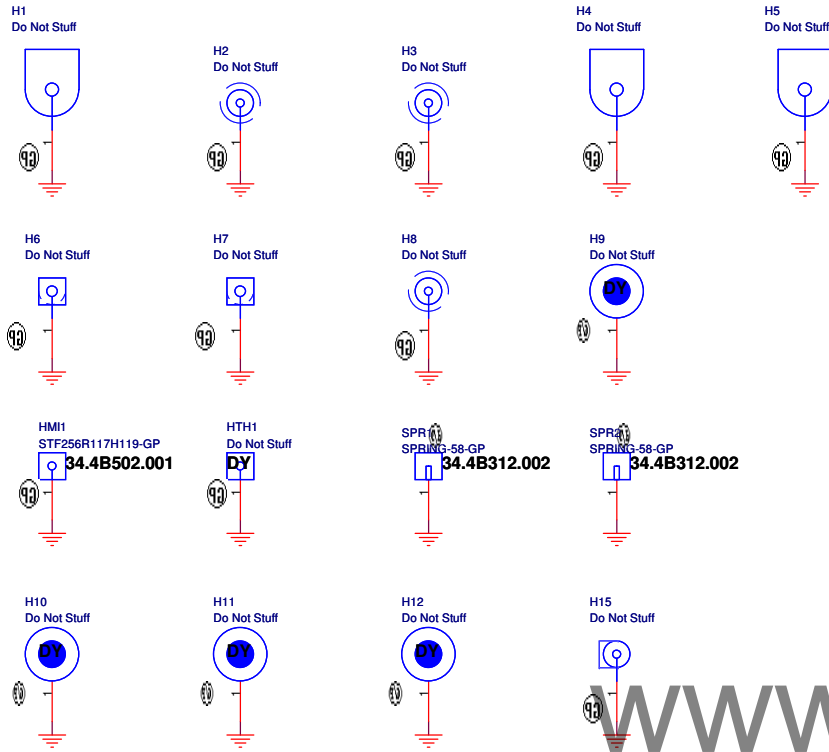
Size  
A3

Document Number  
**Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

Rev  
**A00**

Sheet 78 of 99



DV15 CP UMA second

SSID = VIDEO

www.aitech1.ru

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size

**A3**

Document Number

**Enrico/Caruso 15 CP**

Rev

**A00**

Date: Friday, April 08, 2011

Sheet 80 of 99

www.aitech1.ru

DV15 CP UMA second

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size <b>C</b>	Document Number <b>Enrico/Caruso 15 CP</b>	Rev <b>A00</b>	
Date: Friday, April 08, 2011		Sheet 81	of 99

www.aitech1.ru

DV15 CP UMA second

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
<b>A2</b>	<b>Enrico/Caruso 15 CP</b>		<b>A00</b>
Date:	Friday, April 08, 2011	Sheet	82 of 99

www.aitech1.ru

DV15 CP UMA second

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size <b>C</b>	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011		Sheet 83 of	99

www.aitech1.ru

DV15 CP UMA second

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
<b>Custom</b>	<b>Enrico/Caruso 15 CP</b>		<b>A00</b>
Date:	Friday, April 08, 2011		Sheet 84 of 99



www.aitech1.ru

DV15 CP UMA second

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
Custom	<b>Enrico/Caruso 15 CP</b>		<b>A00</b>
Date:	Friday, April 08, 2011		Sheet 85 of 99

www.aitech1.ru

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size	Document Number	Rev
A3	<i><b>Enrico/Caruso 15 CP</b></i>	<i><b>A00</b></i>

Date: Friday, April 08, 2011	Sheet 86 of 99
------------------------------	----------------

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size  
A3

Document Number  
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Rev  
A00

Sheet 87 of 99


www.aitech1.ru

DV15 CP UMA second

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipen Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size C	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
Date: Friday, April 08, 2011		Sheet 88	of 99

www.aitech1.ru

DV15 CP UMA second



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

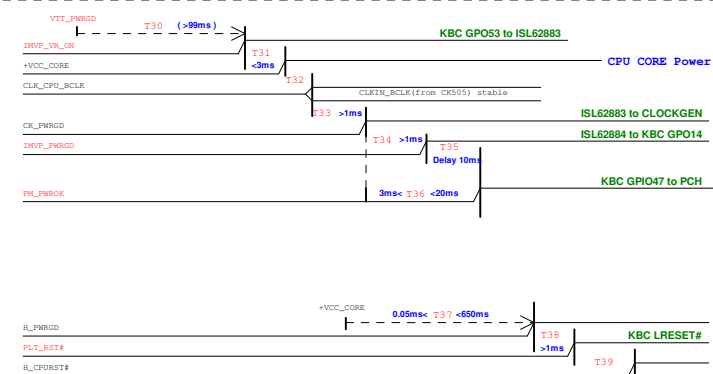
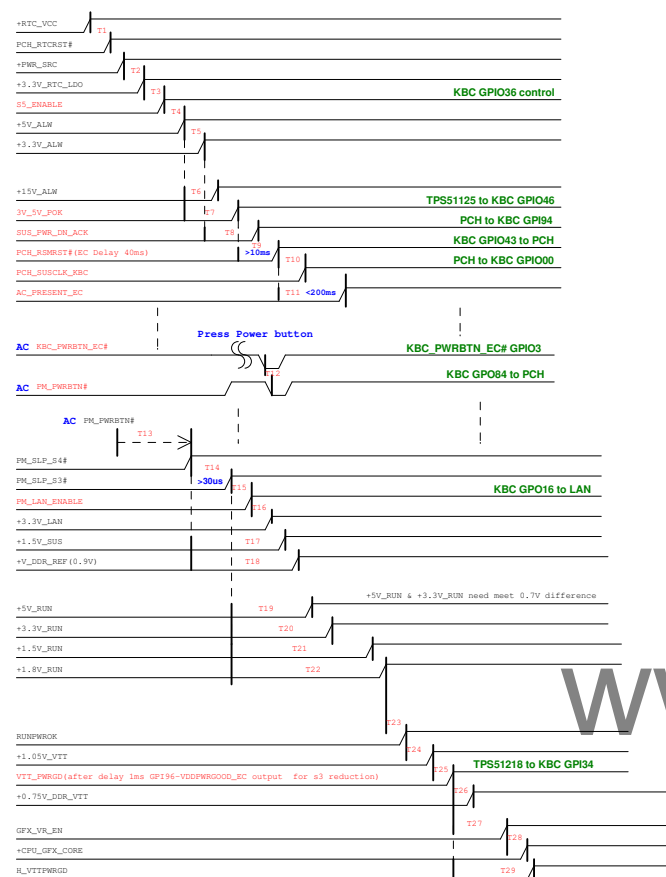
***Reserved***

Size A3	Document Number <b>Enrico/Caruso 15 CP</b>	Rev <b>A00</b>
------------	---	-------------------

Date: Friday, April 08, 2011	Sheet 89 of 99
------------------------------	----------------

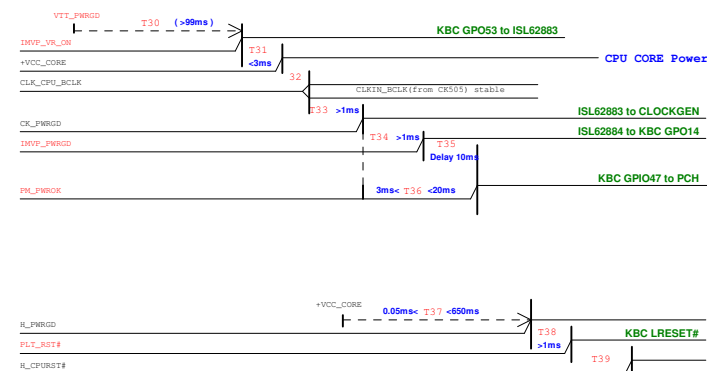
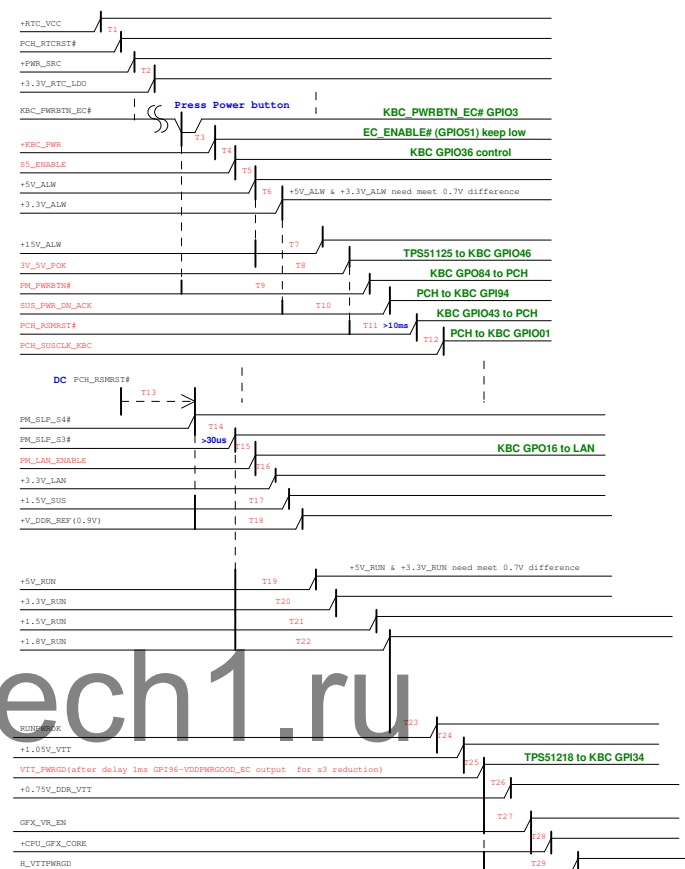
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



Item	Pg.	Date	Description	Owner
KBC	37	A00-0412	stuff R3722 and DY R3725 for change MB version from X02 to A00	EE
WLAN	64	A00-0412	change R6415 from short pad to 0 ohm for debug	EE
USB	54, 63	A00-0412	Remove colay pad(R5403,R5404,R6315,R6316,R6317,R6318,R6319,R6320) after A00	EMI
USB	32, 64	A00-0412	Remove colay pad(EL3201,EL6401) and short pad(R3204,R3205,R6401,R6402) after A00	EMI
CLK GEN	7	A00-0412	change R710~R717 from 0 ohm to short pad	EMI
HDMI	57	A00-0412	Remove colay pad(EL5701,EL5702,EL5703,EL5704) after A00	EMI
short pad	ALL	A00-0412	change PR4519,PR5006,PR5111,R3202,R3742,R3743,R3744,R7105 from 0 ohm to short pad	EE
RTC	62	A00-0412	change U6203 P/N to 83.R0304.B81 for RTC detect leakage issue	EE
RT8237A_+1.05V	49	A00-0412	update PU4901 symbol for part manager footprint change	POWER
WLAN	64	A00-0412	add and DY R6416 0 ohm for Wimax future	EE
POWER GAP	ALL	A00-0413	change power GAP(PG4511,PG4602,PG4604,PG4605,PG4606,PG4615,PG4617,PG4619,PG4621,PG4624,PG4625,PG4607,PG4608,PG4609,PG4622,PG4626,PG4627,PG4610,PG4611,PG4612,PG4613,PG4614,PG4616,PG4618,PG4620,PG4902,PG4903,PG4904,PG4905,PG4906,PG4908,PG4910,PG4911,PG4913,PG4915,PG4917,PG4919,PG4925,PG4926,PG4920,PG4927,PG4928,PG4929,PG4909,PG4901,PG4912,PG4914,PG4916,PG4918,PG5001,PG5012,PG5002,PG5003,PG5004,PG5008,PG5009,PG5010,PG5011,PG5013,PG5015,PG5016,PG5017,PG5104,PG5106,PG5301,PG5303,PG5305,PG5308,PG5311) P/N from ZZ.CON2d.XXX to ZZ.CLOSE.001 for PSE requests	POWER
Thermal	39	A00-0422	stuff R3904 to change T8 temperature setting for reliability test	EE

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size  
A3

Document Number

Enrico/Caruso 15 CP

Rev

A00

Date: Friday, April 22, 2011

Sheet 91 of 99





Item	Pg.	Date	Description	Owner
www.aitech1.ru				

DV15 CP UMA second

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Change History**

Size  
A3

Document Number  
**Enrico/Caruso 15 CP**


Rev  
**A00**

Date: Friday, April 08, 2011

Sheet 93 of 99

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011

Sheet 94 of 99

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 95 of 99	1

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011

Sheet 96 of 99

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History


Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011

Sheet 97 of 99

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History


Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011

Sheet 98 of 99

www.aitech1.ru

DV15 CP UMA second



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011

Sheet 99 of 99